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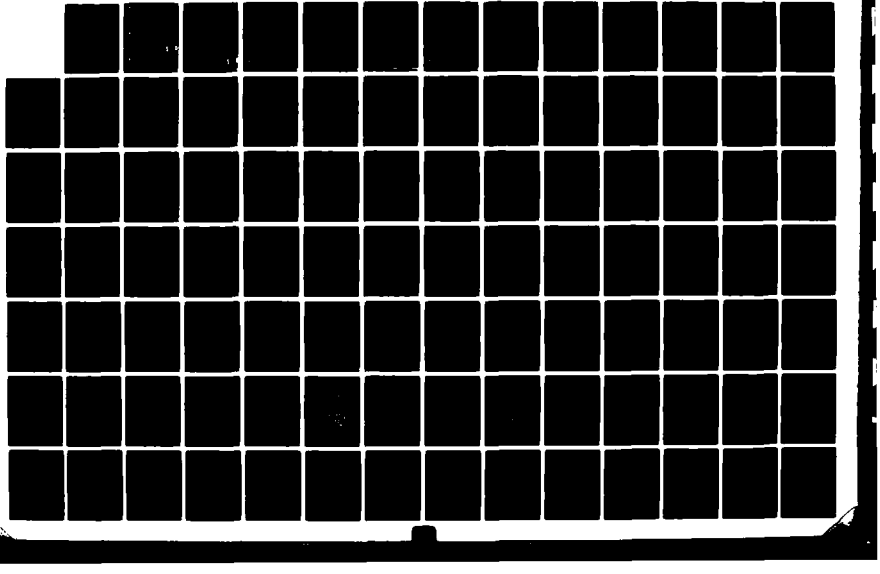

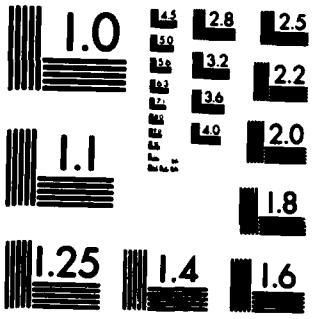

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A PORTABLE PHYSIOLOGICAL DATA RECORDER USING MAGNETIC BUBBLE MEMORY

THESIS

AFIT/GE/EE/83M-2 GROVER R. SIMS
Major USAF

DEPARTMENT OF THE AIR FORCE
AIR UNIVERSITY (ATC)
AIR FORCE INSTITUTE OF TECHNOLOGY

Wright-Patterson Air Force Base, Ohio

AFIT/GE/EE/83M-2

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Approved for public release; Distribution unlimited

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A PORTABLE PHYSIOLOGICAL DATA RECORDER USING MAGNETIC BUBBLE MEMORY

THESIS

Presented to the Faculty of the School of Engineering
of the Air Force Institute of Technology
Air University
in Partial Fulfillment of the
Requirements for the Degree of
Master of Science

by

Grover R. Sims, B.S.E.E., M.A.
Major USAF

Graduate Electrical Engineering
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Preface

This thesis designs a microprocessor driven portable data recorder which uses magnetic bubble memory. The effort builds on previous work to yield a very complete design.

I am deeply indebted to many people across the Air Force who helped me to reach the goals of this thesis. Specifically, I would like to thank Lieutenant Shackford and the USAF School of Aerospace Medicine for funds. I sincerely thank the personnel of the Air Force Avionics Laboratory. Tom Herbert who authorized our use of the computer aided design tools, and Airman Greg Creech who spent a month of effort to layout the microprocessor board deserve special recognition. The coop student Mike Powell and Larry Callaghan each spent a week on the microprocessor board. Mike West and S.E. Cummins provided Magnetic Bubble Memory support.

In AFIT, School of Engineering, Orville Wright and Robert Durham provided valuable expertise and willingness to find and timely procure those ever elusive parts. Thanks to Major Walt Seward, Dr. Mathew Kabrisky, and Captain Larry Kizer for their invaluable guidance as committee members.

Finally, I wish to acknowledge the special support provided by my family. My wife, Sue, placed her own career

on hold to travel with me to Ohio and work for AFIT. Along with Sue, my children Thomas and Laurel have sacrificed time with me so that I could study. I look forward to graduation so that I can spend more time with them.

Contents

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List of Abbreviations

AFIT	US Air Force Institute of Technology, Wright-Patterson AFB OH
A/D	Analog-to-Digital
BACK*	Bus Request Acknowledgement Signal (active low)
BREQ*	Bus Request Signal (active low)
CAD	Computer Aided Design
CLK	System Clock
CMOS	Complementary Metal Oxide Semiconductor
CS*	Chip Select (active low)
DARPA	Defense Advanced Research Projects Agency
DIP	Dual Inline Package
EEPROM	Electrically Erasable Programmable Read Only Memory
EPROM	Erasable Programmable Read Only Memory
FF	Flip-Flop
g	Force of Gravity at Sea Level
GND	Electrical Ground
GUA	Gate Universal Array
IFPDAS	Inflight Physiological Data Acquisition System
IC	Integrated Circuit
INTA*	Interrupt Acknowledge (active low)
INTR*	Maskable Interrupt (active low)

IO/M*	Type of Machine Reference; High signal implies access to input/output device, low implies memory access.
LCC	Leadless Chip Carrier
LSI	Large Scale Integration
MBM	Magnetic Bubble Memory
MOS	Metal Oxide Semiconductor
MOSFET	MOS Field Effect Transistor
MOSIS	MOS Implementation Service
MSI	Medium Scale Integration
MTBF	Mean Time Between Failures
MTTF	Mean Time to Failure
NAND	Negated "AND" Function
NMI*	Non-Maskable Interrupt (active low)
NMOS	Negative Channel Metal Oxide Semiconductor
PAL	Programmable Array Logic Device
PCB	Printed Circuit Board
PROM	Programmable Read Only Memory
RAM	Random Access Memory
RD*	Read Strobe (active low)
RFSH*	Dynamic Memory Refresh Signal (active low)
ROM	Read Only Memory
RSTx*	Maskable Interrupts, x = A, B, or C (active low)
SSI	Small Scale Integration
S0, S1	Microprocessor Machine Cycle Status

TTL	Transistor-Transistor Logic
USAFSAM	US Air Force School of Aerospace Medicine, Brooks AFB TX
VLSI	Very Large Scale Integration
WR*	Write Strobe (active low)
XWAIT*	Processor Wait Request Signal (active low)

Abstract

Text documents the physical design of a man-portable digital data acquisition system. Work includes schematics and detail part drawings. The design is essentially a single board computer featuring all CMOS parts. Secondary storage is on a mixed technology board which includes an Intel 7110 magnetic bubble memory device.

A Portable Physiological Data Recorder Using Magnetic Bubble Memory

I Introduction

Problem Statement

One aspect of the Air Force mission is to safely place airmen in aircraft. The AF engineer who designs equipment to aid in this task must accumulate and evaluate information gathered to quantifiably measure equipment success. The Air Force needs a device which will record the physiological condition of airmen and the environmental condition of a cockpit. Currently, a cassette tape recorder which collects data on an analog tape format is used; however, studies (15) have proposed a digital device which would use low power integrated circuitry to analyze and compress the sensor data and store the conditioned data in a magnetic bubble memory. In effect, the device would be a small computer which would have a central processor, input and output sections, and memory. The recorder must be rugged, lightweight, and not impede the movement of the host aircrew member.

Other scenarios can be envisioned for the use of such a device. Parachute jumpers could serve as hosts for the device. Military agencies interested in the development of chemical, biological, and nuclear protection garb may be interested in physiological data.

Limits of Problem

The recorder must operate from a self-contained battery and be free of wires between it and the aircraft. This

requirement results from safety, economy, and convenience considerations.

The crew members in many DOD aircraft are protected by an emergency egress system, usually a rocket powered ejection seat. Any wire between an ejecting crew member and the aircraft must separate, without undue stress on the crew member. Cables could be designed to alleviate the problem, but the sure way to avoid the problem is to eliminate any wires between the recorder and the aircraft.

The self contained concept avoids expensive aircraft modification. When attempted, aircraft modifications complicate aircraft maintenance and must be closely scrutinized to insure that personnel and equipment safety are not jeapordized. The self-contained recorder design avoids aircraft modifications.

The recorder is convenient to use if aircraft modification and most safety issues are avoided by being self contained. If the recorder required an aircraft modification for each test flight, the recorder would be inconvenient to use and simply would not be used by the testing office because of the administrative burden. The data would remain unrecorded or be recorded in a less satisfactory way.

The battery should have the capacity to operate the recorder over the period of a typical test flight, and the recording must retain the stored information long after power is removed. Few test missions exceed four hours in

length but many run less (20). Thus, four hours was chosen as the typical mission length. When a mission is longer than the battery life, the host crew member will be busy with flying duties, and the recorder must shut down automatically and retain the data that it has collected.

The recorder must be rugged in order to be reliable under expected bouncing and jostling. At the check out site, the equipment will experience shock and vibration during the transport from the check out site to the flight line where it will meet its host. The recorder may be exposed to temperature extremes, sunloading, precipitation, salt spray, and humidity. During flight, the recorder must operate properly during high-g maneuvers and in the cockpit environment.

The recorder must be maintainable in order to return it to service quickly when a failure does occur. A very elegant device can be realized in this institute's laboratories, but it may be unrepairable with the tools and skills found in the flight test laboratory. The recorder designer should consider supplying maintenance tools and maintenance instructions along with the recorder hardware.

The recorded data must survive power loss due to battery drain from long missions. Further, if a battery fails during a mission the data recorded to that point must survive. Very "interesting" data may be collected near an unexpected battery disconnect, and this data must not be

lost. An unexpected battery disconnect implies that the recorder may have experienced abnormal stress levels, and physiological reactions to this unexpected condition should be of scientific interest.

Significance of Problem

A mission of the United States Air Force School of Aerospace Medicine is to develop effective life support systems for high performance aircraft. One aspect of this mission is the collection of environmental and physiological data during aircraft flight. This data then becomes the history which future life support systems are judged against.

A trend in warfare preparation in the world today is chemical, biological, and nuclear defense. The Air Force is developing life support garments for these environments. This mission, too, requires the collection of environmental and physiological data during duties in these garments. The recorder must be self contained in these applications.

History of Problem

The School of Aerospace Medicine currently collects inflight data using the Inflight Physiological Data Acquisition System (IFPDAS)(Fig 1). Since IFPDAS is the primary system for data acquisition, it is an important system for evaluation of Air Force life support systems. The IFDAS uses an analog cassette recorder to record data on

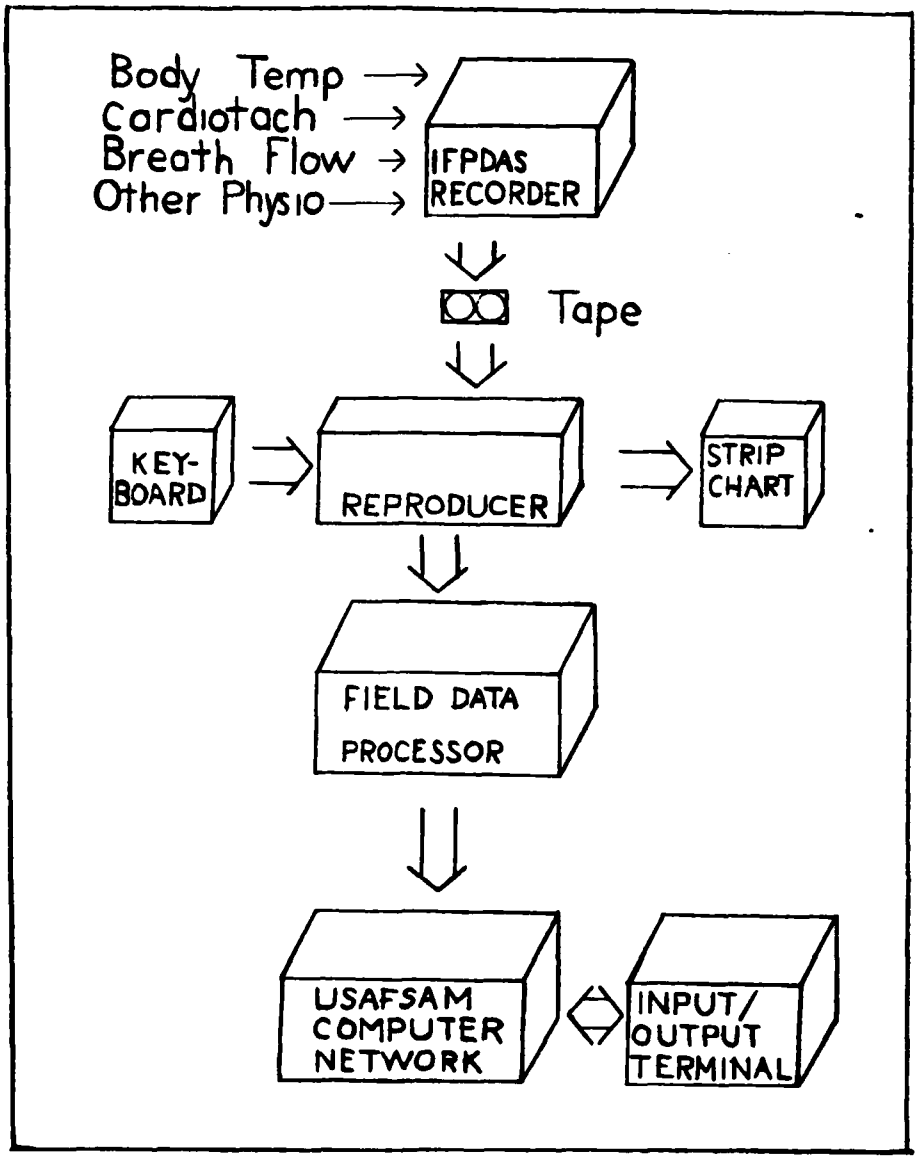


Figure 1. Inflight Physiological Data Acquisition System Block Diagram

such items as pilot voice, electrocardiogram, cabin pressure, oxygen consumption, expired flow, and vertical acceleration. IFPDAS is a data collection system that performs the functions of data collection, field data processing, and computer aided data manipulation.

The data collection function requires transducers to convert physical phenomena to electrical signals. IFPDAS transducers include an electrocardiogram amplifier and tachometer, an inspired and expired breath flow monitor, an oxygen content monitor, an absolute pressure transducer, an accelerometer, and an audio amplifier. Spare channels are available to connect other physiological and environmental data sensors. All signals are conditioned and time multiplexed by three eight channel analog multiplexers. The multiplexed signals are recorded using a pulse duration modulation format by the flight recorder. This thesis proposes replacing the flight recorder but retaining the existing transducers.

Field data processing of the IFPDAS is accomplished by the data reproducer, field data processor, and a strip chart recorder. Field processing capability allows test personnel to insure that the data collection system is operating properly at the final oportunity before initiating the test mission. Often this is at the flight line.

The field data processor is a microcomputer which is used for a simple analysis of data and a quick check of results in the field. The field data processor contains 24k

bytes of random access memory (RAM) and 11k bytes of erasable programable read only memory (EPROM).

The data reproducer is contained in a rugged aluminum suitcase and converts the pulse duration modulation signals on cassette tape to time varying analog signals. The reproducer contains a microprocessor, a timing decoder, a binary coded decimal converter, and three signal integrators. The reproducer can search for a specific time segment and data segment. The data is then displayed by a strip chart recorder.

The present IFPDAS data recorder has major characteristics which can be altered in a favorable way through this thesis approach: high-g loading on the cassette drive mechanism, degree of difficulty to change signal inputs, characteristics of analog recordings, and maintainability considerations.

Early versions of the IFPDAS flight recorder drive mechanism labored under high-g's and this data was lost. High-g periods are the critical times when the data is especially interesting, because the physiological effects of high-g maneuvers could yield clues through emotionally and physically induced changes in data. High-g periods include dog fight maneuvers, emergency scenarios, and abnormal operation conditions.

The latest version of the IFPDAS recorder has a cassette drive which is purported to operate under high-g loading, but that device has not been flown by the USAFSAM (20). Reguardless of the validity of the claim, replacing

the mechanical drive with a totally solid state memory holds potential dividends in reliability, mechanical ruggedness, and cost.

The present IFPDAS recorder suffers from the inflexibility to modification which is characteristic of hardware designs.

History of Past Attempts

Jolda and Wanzec (13) assembled hardware and software for a microprocessor based prototype data recorder. Their hardware consisted of an Intel SBC 80/20 single board computer, an Analog Devices DAS 1128 data acquisition module, various transducers, and an interface for mass data storage. They proposed a bubble memory for mass data storage.

The next year Hill (9) studied system requirements and conceptualized a design approach.

In 1980 Moore (19) proposed an architecture for a data aquisition recorder that would sample and hold 12 environmental and physiological measurement signals. He conceptualized a one-megabyte Intel magnetic bubble system for primary storage. Hill's selection of Intel over the US competition of the time was fortuitous because, today, only Intel makes bubble memories in the US. He also investigated data storage algorithms.

Meisner (15) continued these efforts and finalized the new recorder architecture. He proved his design with a breadboard demonstration unit.

Accomplishments of Past Work

The previously mentioned thesis efforts have established that a small, rugged recorder can be built using CMOS digital circuitry and a magnetic bubble memory (MBM). These authors have written some software and built test circuitry which demonstrates the general utility of the approach.

Meisner went further than the rest. He provided an architecture based on CMOS and MBM technologies. The microprocessor set used is the NSC800 supported by an MM82PC12 demultiplexer and an NSC810 RAM\IO\timer. The resident operating system is contained in Hughes HNVM3008 EEPROMs and Hitachi HM6116 RAMs provide temporary storage. When temporary storage is full, data is transfered to an Intel magnetic bubble memory system.

Areas for Continuing Effort

While past efforts are encouraging, they stop short of a design which meets quantified values for electrical function, weight, volume, reliability, and maintainability. Further, software needs to be developed to efficiently store and retrieve data. Finally, an interface must be designed and built to move data from the bubble to a quick check device on the flight line and to a mainframe computer such as the PDP11-70 at USAFSAM.

Scope of Effort

This thesis designs and builds an inflight recorder with the mechanical, functional, and reliability qualities needed to satisfy USAFSAM requirements for an inflight

recorder. The device will incorporate recent advances in complementary metal oxide semiconductor technology (CMOS) which make possible dense electronic circuits with very low power and size requirements; and magnetic bubble memory technology, which provides dense, nonvolatile memory. The recorder will use a microprocessor which allows the mix of signal inputs to be simply modified through software changes and without difficult hardware modification. Data will be converted from analog to digital format which improves noise immunity and signal drift.

Sequence of Presentation

This thesis is organized chronologically beginning with the conception of the need for the product and then continuing on to its design requirements, product design, and design evaluation. This chapter has reported on the perceived need for an improved recorder and the history of past attempts to build one. The next chapter establishes the need to define the proposed recorder in quantifyable and discrete terms, and continues on to establish the requirements in measurable terms.

Chapter III reports on the approaches that were considered to build the recorder. The ways considered include custom integrated circuits, hybrid circuits, dual inline packages, leadless chip carriers, and batteries. Each technologhy is defined in relation to the recorder and evaluated against the design requirements and constraints.

The success of the design which is described in Chapter

III must be judged by how well the product satisfies the design requirements of Chapter II. To that end, Chapter IV describes an evaluation plan which is used to measure design success.

Finally, Chapter V summarizes the work done by this thesis and outlines the tasks that remain to be accomplished by future investigators.

II Design Requirements

Overview of Electronic System Design

Electronic system design can be viewed as a chronological series of events. First a concept is hypothesized as a solution to a problem or as a better solution than previously implemented. For example, optical fiber technology has replaced copper wire in many applications because fibers weigh less and have a higher bandwidth in a given cross section than copper conductors (29:42,4). The next event in the design process is analysis to evaluate potential performance gains, cost advantages, and technical risk contained in the hypothesis. This analysis may include exploratory development work in an applied laboratory environment.

If the decision maker is willing to accept the risk of development after considering the potential benefits disclosed by the analysis, the product enters the preliminary design stage. During this time the requirements and objectives are formally established, and a design approach is selected, the product is partitioned into subproducts, the electrical design is schematically diagrammed, and the physical properties are reduced to drawings and analytically described. At the end of this period the decision maker can again review the product to determine if the next design stage should be entered. More information is available now to update earlier analysis, and calendar time has elapsed. Perhaps a technological

breakthrough has been reported elsewhere which makes the benefit of the developing product less attractive or competative products have developed.

The next stage of product development is detailed design. Assembly drawings and detail drawings are produced to describe the product and each subproduct. A prototype is built and tested in the laboratory. Results from laboratory tests are incorporated into the prototype design and the product is ready to enter the field.

The product matures as user experience is incorporated into production unit changes and the builder optimizes the manufacturing costs, technical performance, and delivery schedule.

Finally, the product design obsolesces because the need for the product diminishes or emerging technologies fill the need in a better fashion.

This thesis effort accepts the analyses and preliminary design of the previously cited theses efforts and continues the effort into detailed design.

System Requirements

The purpose of an electrical system development is to perform an electrical function; however, detailed technical requirements are rarely clear. Technical obsolescense, emerging technologies, competition, and the needs of the end user are constantly changing to produce an ever shifting requirement base. In spite of the difficulty, system requirmements must be formalized as well as possible.

The formal requirements provide a focus for all aspects of the development, and they provide a standard against which the developing product is evaluated.

The device shall record the physiological parameters found in Table I and the environmental sensors listed in Table II.

Table I. Physiological Sensors (21:8)

	Parameter	Measurement Range
a.	inspired flow rate,	0-240 liters/min
b.	expired flow rate,	0-160 liters/min
c.	inspired oxygen concentration,	0-760 mmHg
d.	exspired oxygen concentration,	0-760 mmHg
e.	body temperature,	20-50 degrees C
f.	heart rate (19:3).	50-200 beats/min

Table II. Environmental Sensors

	Parameter	Measurement Range
a.	triaxial acceleration,	±25 g
b.	cabin pressure,	0-15 psia
c.	anti-G suit pressure,	Not Specified
d.	mask pressure (19:3).	Not Specified

The heart rate sensor provides an analog signal and an associated eight-bit digital word. Each of the other sensors listed previously provides a 0-5 volt analog signal.

None of these sensors is accurate to better than 1%, thus 1% accuracy is suitable for the new recorder.

Electrical requirements

The recorder shall be solid state. The recorder shall have provisions for 16 sensor inputs and, it shall measure at least 122 samples per second. The recorder shall operate with a battery for four hours (15:8).

Electric Interface

The sensor connector shall be a Cinch type DF-50 or equivalent and pin functions shall be as described in Table III.

Human Factors

Flexibility for Change. Requirements shift with the passage of time because of advances in technology, user needs, and changing cost pictures. The ultimate obsolescence of an electrical system can be delayed by considering the flexibility for change during its design. It is expected that additional requirements will be identified in the future. For example (19:4) USAFSAM personnel express interest in various real time processing techniques for electrocardiograms.

The recorder shall be microprocessor controlled (15:10) so that modification can be implemented through software. The recorder shall have ports for input and output.

Table III. Sensor Pin Functions

Pin No.	Signal & Type	Active Level	Description
1	GND	L	Common with pin 20
2	STB	L	Strobe input from sensors
3	PA0		Bit 0 of 8-bit input/output port A, LSB
4	PA1		Bit 1
5	PA2		Bit 2
6	PA3		Bit 3
7	INTR	L	Strobe mode interrupt request to CPU
8			Reserved for EEPROM write signals
9			"
10			"
11			N/C
12			N/C
13			N/C
14			N/C
15			N/C
16			N/C
17			N/C
18			N/C
19			N/C
20	GND		Common with pin 1
21			Bit 7 of 8-bit input/output port A MSB
22			Bit 6
23			Bit 5
24			Bit 4 of 18-bit input/output port A
25	BF	H	Buffer full output to sensors
26	+5 volts		Common to pin 44
27	IN0		Sensor no. 0, 0-5 volt analog signal
28	IN2		Sensor no. 2, 0-5 volt analog signal
29	IN4		Sensor no. 4, 0-5 volt analog signal
30	IN6		Sensor no. 6, 0-5 volt analog signal
31	IN8		Sensor no. 8, 0-5 volt analog signal
32	IN10		Sensor no. 10, 0-5 volt analog signal
33	IN12		Sensor no. 12, 0-5 volt analog signal
34	IN14		Sensor no. 14, 0-5 volt analog signal
35	IN1		Sensor no. 1, 0-5 volt analog signal
36	IN3		Sensor no. 3, 0-5 volt analog signal
37	IN5		Sensor no. 5, 0-5 volt analog signal
38	IN7		Sensor no. 7, 0-5 volt analog signal
39	IN9		Sensor no. 9, 0-5 volt analog signal
40	IN11		Sensor no. 11, 0-5 volt analog signal
41	IN13		Sensor no. 13, 0-5 volt analog signal
42	IN15		Sensor no. 15, 0-5 volt analog signal
43	VDD		EEPROM power
44	+5 volts		Common to pin 26

Physical Characteristics. The recorder shall be totally portable with no wires from the host to the environment (15:8), and small enough not to encumber movement. The recorder shall measure 2X5X9 inches (19:59).

Reliability

The recorder shall resist failures (15:8). Reliability is the probability that an item will perform its intended function under stated conditions for a stated time period. The designer would like to predict reliability during the analysis and design periods of product development, and fortunately, analysis techniques exist which predict reliability of electronic systems during development design periods. Before an analysis can be performed, certain terms must be defined.

The "required function " in the reliability definition of the flight recorder includes the performance specified in this chapter, along with the criteria for failure. Failure is not as obviously defined as casual reflection may expect. For example, the flight recorder samples physiological data which changes very slowly compared to the clock period of a microsecond. A human at rest may complete a dozen respiration cycles in sixty seconds. One or two bad data samples recording respiration rate in a long string of valid data do not consititute a failure. For the sake of analysis here, the recorder is operating properly if 80% of the expected information is recorded properly.

The mission cockpit environment are the stated conditions for the recorder. The cockpit environment was

considered when the physical environment section of this chapter was written. Environmental requirements for this type of AF equipment are often defined by MIL-E-5400. The "stated period of time" is four hours which is the operating period previously stated.

Often the term availability is associated with reliability. Availability is defined as "the probability that an item will operate when needed." This concept considers that an item must be unavailable from the time a unit fails until it is repaired. This concept is very useful for items such as commercial communication links, but is is not useful for the flight recorder, where a failure cannot be repaired during the four-hour mission duration; therefore, the concept of availability will not be considered for the flight recorder.

The exponential probability distribution is extensively used for reliability predictions. The exponential probability distribution is given by

$$R(t) = e^{-\lambda * t}, \quad 0 \leq t < \inf \qquad (1)$$
$$= 0, \quad \text{otherwise}$$

where

R(t) is the probability that the item survives until sometime t

λ is a constant

System reliability is often reported as mean time to failure (MTTF)

$$MTTF = \int R(t)dt \qquad (2)$$

If an item operates until it fails and is repaired and returned to service, then the term, " mean time between failures" (MTBF) becomes convenient. If R(t) is independent of the period of operation then MTBF and MTTF have the same meaning. As the operating time becomes very large, MTBF approaches a constant value

$$MTBF = 1/\lambda \qquad (3)$$

System reliability is related to the reliability of each component item in the system. If a system is composed of a series of items with mutually independent reliabilities that are exponentially distributed, then the system reliability is a product of the component systems (6:162). Further, if a system is composed of parallel (redundant) items with mutually independent reliabilities that are exponentially distributed, then the system reliability is given by

$$R(t) = 1 - \sum (1-R_i) \quad (6:151) \qquad (4)$$

where

R(t) is system reliability

R_i is reliability of system "i"

n is number of redundant items

By viewing a system as a network of series and parallel components, a prediction of system reliability can be made. The prospective flight recorder circuit was viewed to clasify components as critical or non critical. Critical components are those whose failure would result in failure of the recorder. The parameter λ for each critical component can be estimated from a study of historical data which has been compiled by the Rome Air Development Center (RADC) (16:). The parameter λ for monolithic MOS devices can be estimated by (16:para 5.1.2)

$$\lambda = Pi_Q[C_1 Pi_T Pi_V + (C_2+C_3))PiPvEPv]Pi_L$$

where

λ is measured in failures per 10^6 hours

Pi_Q is a quality screening factor

Pi_T is a temperature stress factor

Pi_V is a voltage derating stress factor

Pi_E is an environment stress factor

C_1 and C_2 are circuit complexity failure rates

C_3 is a package failure rate factor

Pi_L is a device learning factor

The parameter λ for each critical MOS device was computed using MIL-HDBK-217D (16:) and its value entered in Table IV. For this estimate, it was assumed that each device was procured in full accordance with MIL-M-38510 class B requirements for reliability. The assumed environment was judged to be halfway between a benign laboratory condition

and a soldier's manpacked equipment. Because CMOS does not produce much heat, junction temperatures were estimated at 35 degrees C. The Intel bubble support devices were assumed to have a 45 degree C junction temperature. The Intel 7110 MBM is not an MOS device and its λ parameter was estimated using a recent study (5:29). Critical components were then viewed in a network to disclose their series and parallel relationships. Table IV is a list of critical components.

The memory devices are parallel in the sense that failure of one would leave others operable. The failure of one Hitachi HM6116 RAM memory would leave three still functioning; however, RAM capacity would be diminished to 75% of the designed capacity which is below the failure definition. It was earlier stated that less than 80% of the expected information received constituted a failure. When viewed from this perspective, a failure of a Hitachi HM6116 RAM results in a system failure; therefore, for the purpose of reliability analysis, each HM6116 RAM is considered a series component. Similarly, each Hughes HNVM 3008 EEPROM is considered to be in series. No critical components are identified as in parallel, and the system is viewed as a series circuit of critical components. Using the data in table IV, it is computed that the system λ is 3.7766 failures per 10^6 hours and by equation 4 the system MTBF is 2.65×10^5 hours.

Table IV. List of Critical Components

Component Identifier	Size Pins	λ $f/10^6$ hrs
C1	24	.0467
C2	40	.1068
C4	14	.0250
P10	20	.0341
P11	20	.0341
P12	20	.0341
R13	20	.0341
R14	20	.0341
R15	20	.0341
U16	20	.0341
U17	20	.0341
P19	16	.0294
P20	16	.0294
R21	14	.0236
R22	14	.0236
U23	14	.0236
R24	14	.0236
U25	16	.0294
R26	14	.0236
M	4-24 PIN PACKS	.5453
R40	24	.1905
R41	24	.1905
R42	24	.1905
R43	24	.1905
U50	40	.0982
U51	40	.0982
XU5		.773
XU7	40	.1206
XU2	16	.0290
XU1	14	.2908
XU3	14	.2908
XU6	22	.0518
XU4	20	.0594

This chapter has defined system requirements in concrete and measurable terms. In some areas analytical models have been used to predict the technical risk of selected requirements. In the next chapter the thesis develops the detailed design. The design approach is selected, the recorder is partitioned into modules, and the recorder is finally described in detail.

III Product Design

The thesis evaluated current technologies to determine the best way to build the recorder. Areas considered included computer aided design of printed circuit boards, custom and semicustom integrated circuits, hybrid designs using both thin and thick film photolithographic technologies, battery selection, and discrete component selection.

The recorder electrical design approach was adopted from Meisner (15). The partitioning of the recorder into subproducts depended on the physical design technology which was finally selected. The recorder schematic is shown in Figure 2.

This chapter is organized chronologically so that each technology is introduced in the sequence that it was considered.

Design Constraints

The conceptualization of a physical design must be timely if it is to be practical. Many of the ideas presented herein are aesthetically pleasing, but may depend on procuring components with long delivery lead times. It was decided early in this thesis effort that the thesis should design a recorder that could be built in the spring 1983, even at the expense of more elegant approaches that may have promise for future dates.

It was also realized early on that a custom design of the magnetic bubble memory board was labor intensive and

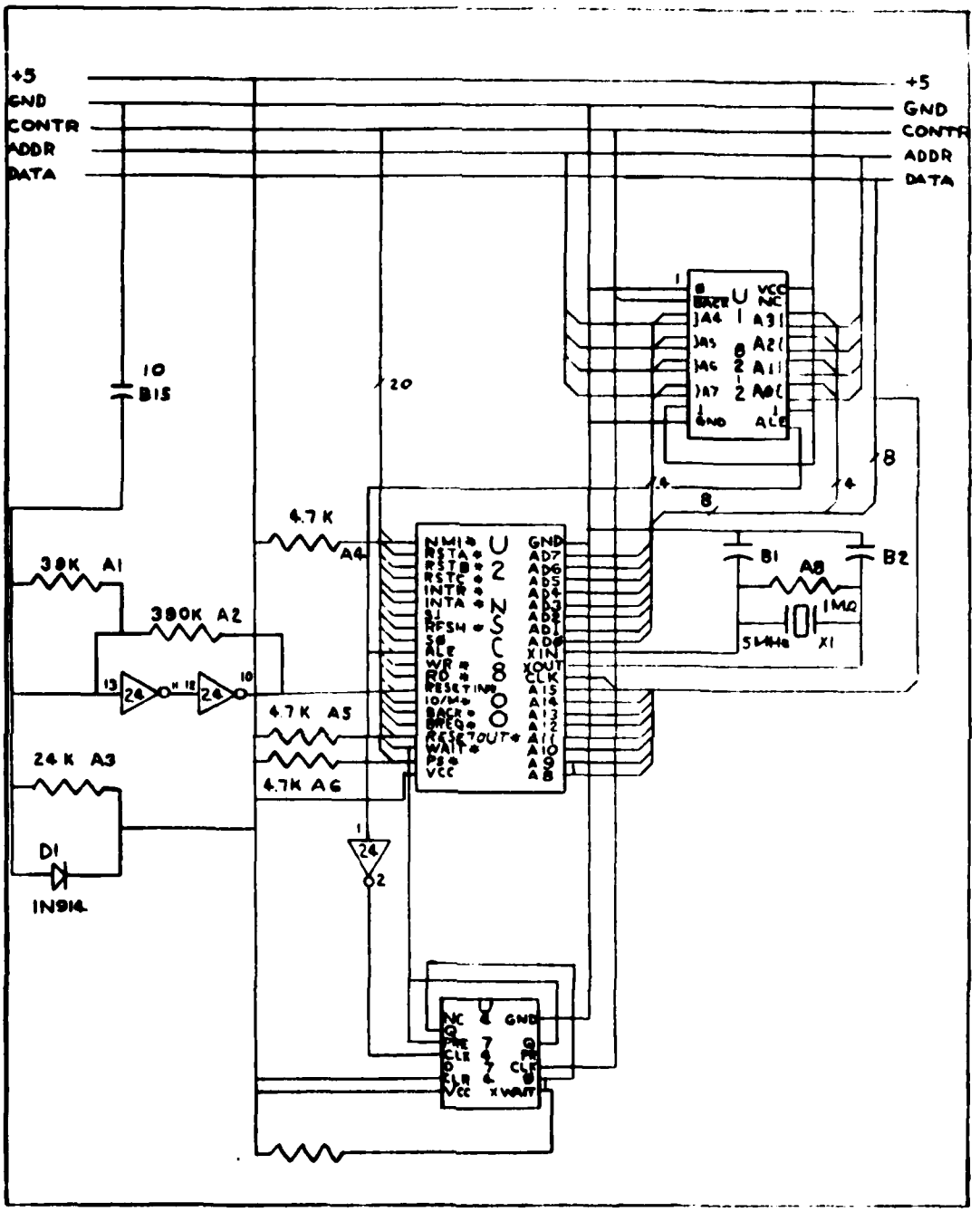


Figure 2. Flight Recorder Schematic (15:94,98)
Sheet 1 of 5

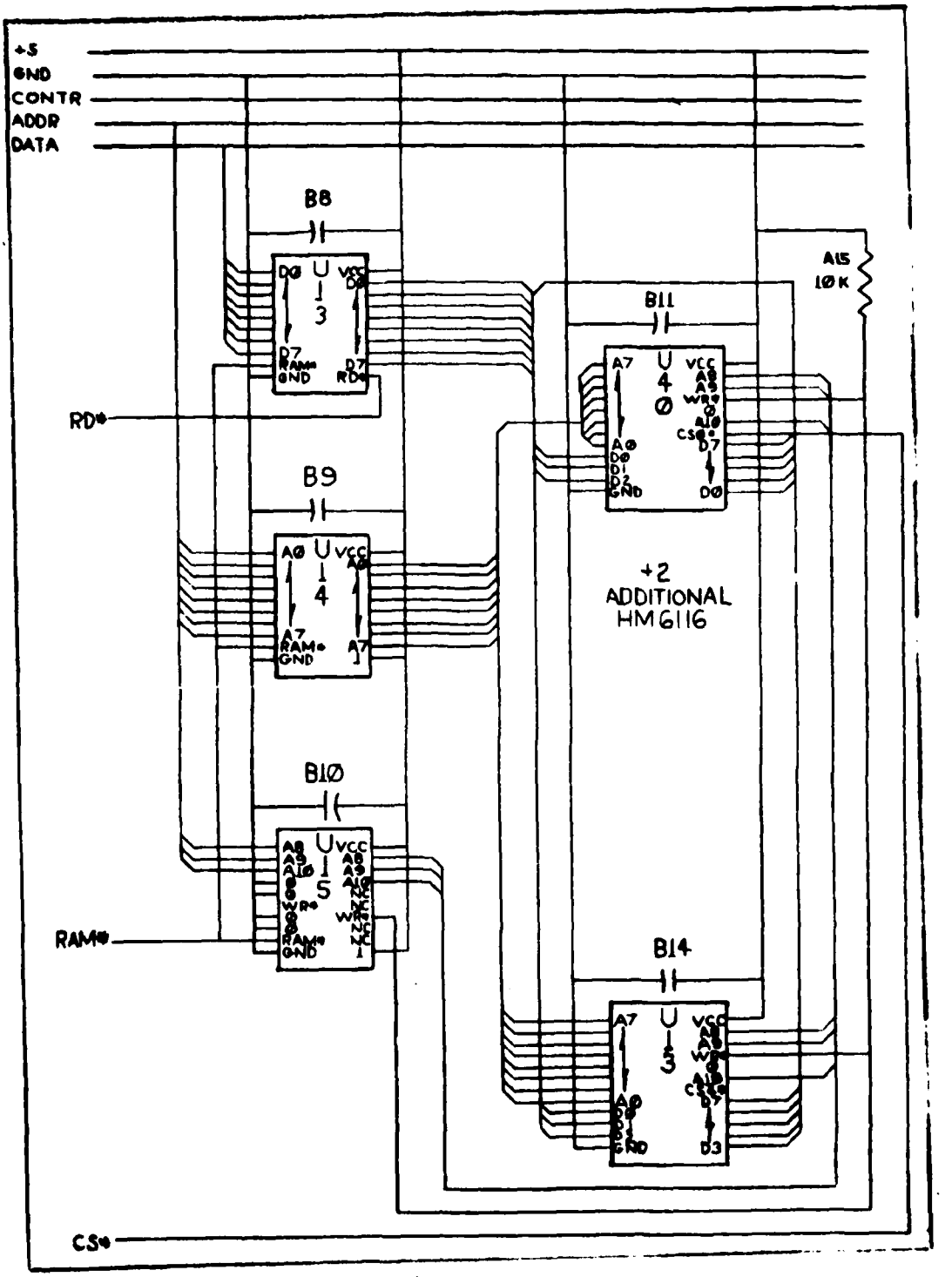


Figure 2. Flight Recorder Schematic (15:94,98)
Sheet 2 of 5

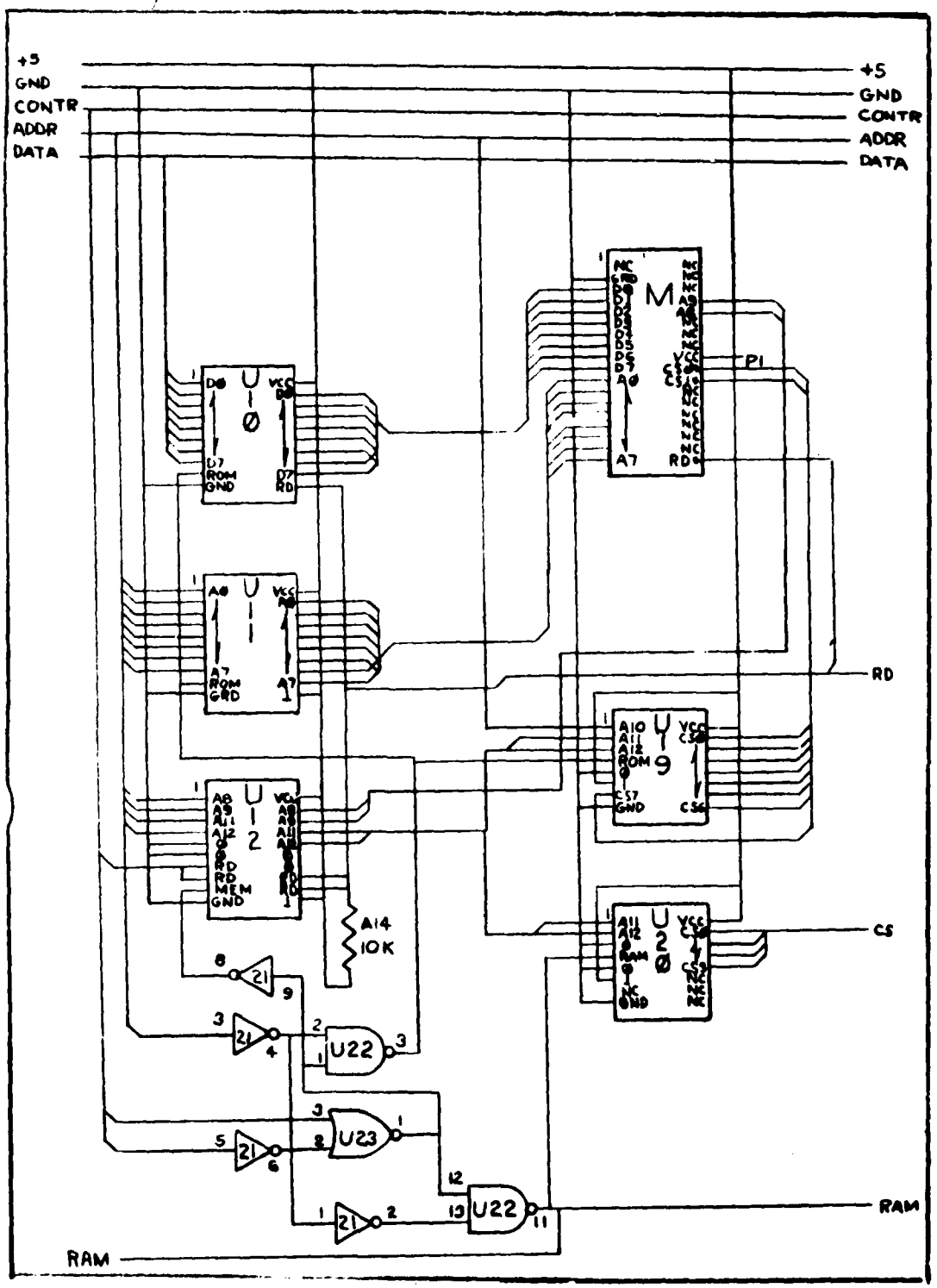


Figure 2. Flight Recorder Schematic (15:94,98)
Sheet 3 of 5

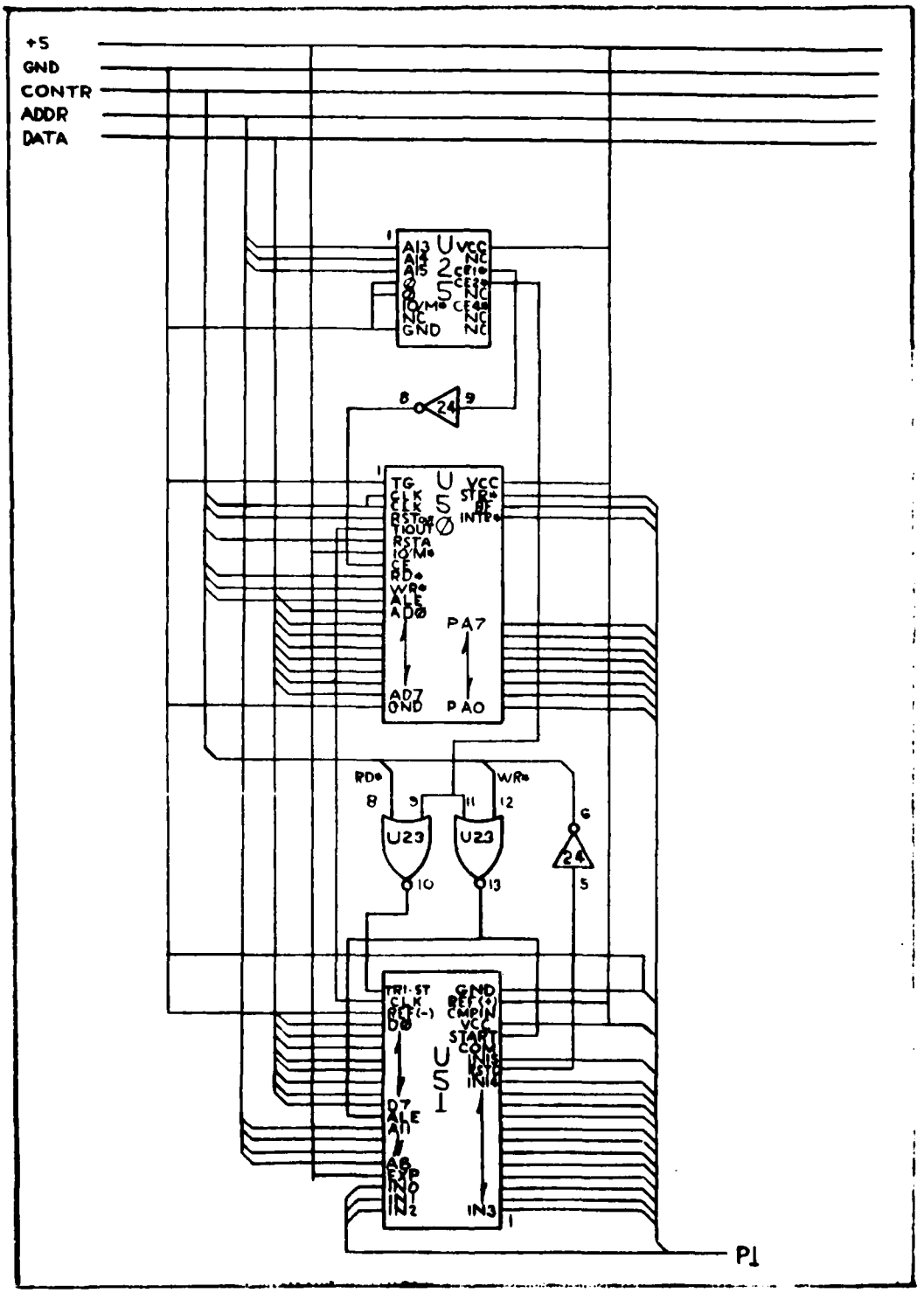


Figure 2. Flight Recorder Schematic (15:94,98)
Sheet 4 of 5

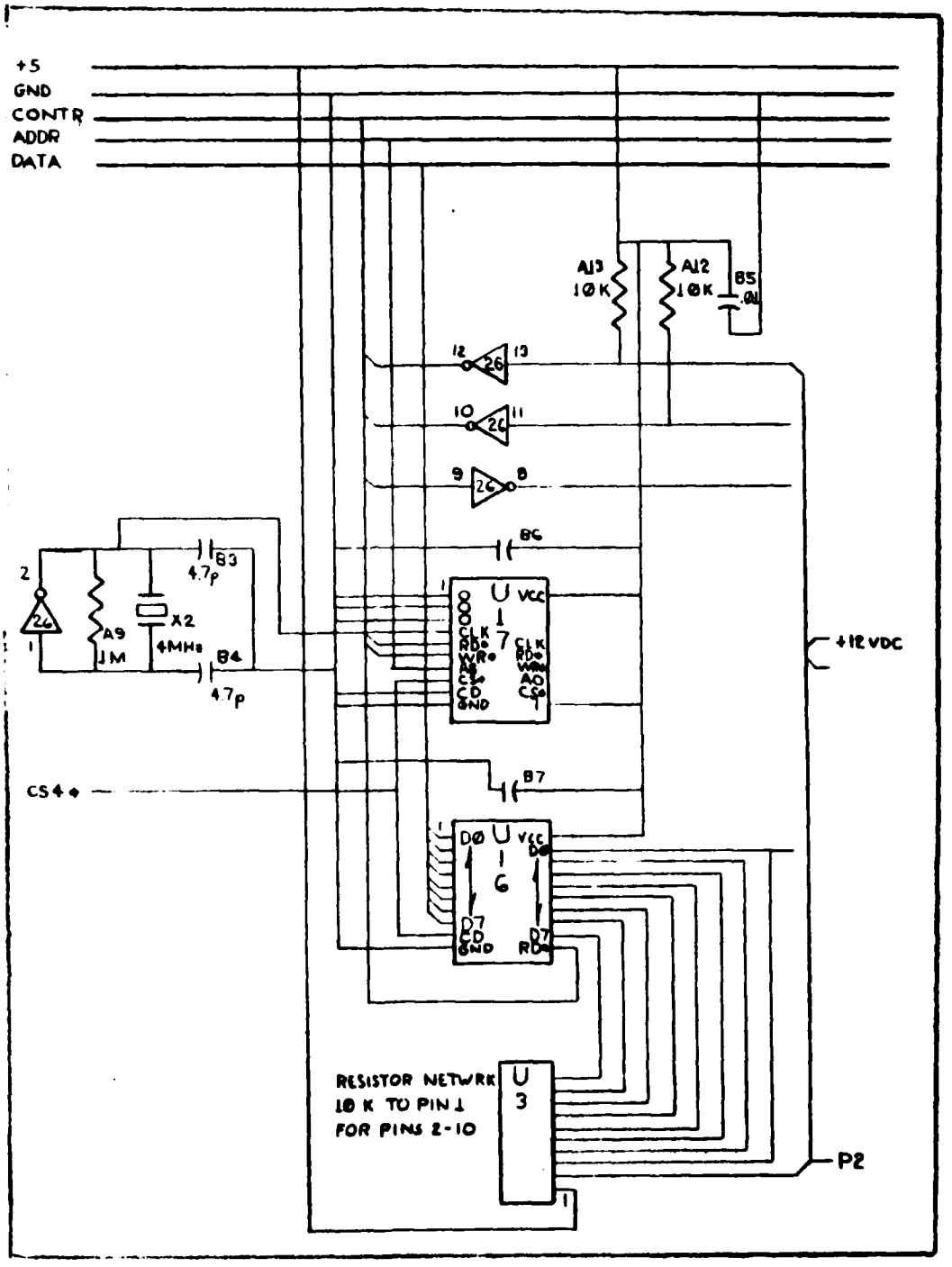


Figure 2. Flight Recorder Schematic (15:94,98)
Sheet 5 of 5

technically risky. For these reasons it was decided that the design would include the Intel BPK 72 which is a production design of a magnetic bubble memory board. Again, this decision was made so that the recorder could be built in the spring 1983.

Hybrid Package

Hybrid circuits are those which are built using both thin film and thick film technologies. Thin film processes use photolithographic techniques to produce resistors, capacitors, and conductors on substrates. Thin films range in thickness from about one hundred angstroms to several microns. Thick film processes use silk screen techniques to produce passive components on substrates which are fired at high temperatures to form the desired films. Thick films are usually an order of magnitude thicker than thin films. The ceramic material alumina (Al_2O_3) is a common substrate material for both technologies (7:346-401).

The full utility of hybrid circuits is realized when thick film conductors are used with appliqued components and silicon integrated circuits. If the components were on hand, a design using hybrid circuits could be produced by this thesis effort using facilities at the AF Avionics Laboratory. Unfortunately, cost and time constraints frustrate the hybrid circuit approach at this time.

Overview of Custom Chip Technology

The recorder is required to be light, reliable, and operate for a long period on battery power. These

objectives lead the digital designer to consider a custom silicon device. Many functions can be placed on a single Large Scale Integrated (LSI) die, and these dice can be produced in quantity very inexpensively using today's LSI fabrication techniques. The object of many of today's LSI designs is to pack a large number of Small Scale Integration (SSI) and Medium Scale Integration (MSI) die-sized functions onto a single LSI die. LSI designs are not layed out automatically, but they lend themselves to computer aids because of the small physical size of the layouts and the complexity of the circuit functions (25:38).

The four basic ways to automate IC layouts are: (1) Standard cell, where a large library of predefined cell descriptions such as NAND gates and counters are stored in the system; (2) gate arrays, which contain rows of identical cells such as NOR gates or individual transistors on a prefabricated wafer; (3) programmed logic arrays, which contain two arrays, one NAND and the other NOR, that in series perform any combinational (not clocked) Boolean function; and (4) standard floor plan, which zones areas of the die for specific functional units, bus, and wiring strategy (25:39).

The thesis evaluated current LSI custom and semicustom capabilities that were available to theses work at AFIT. Candidates included programmable array logic, N-channel Metal Oxide Silicon (NMOS) and Complimentary-Metal Oxide

Silicon (CMOS) custom circuits using the Mead-Conway design methodology (14), and CMOS on a sapphire epitaxial layer (CMOS/SOS) Gate Universal Array (GUA).

Equivalent Gate Complexity

The recorder consists of a microprocessor, special purpose and input/output (I/O) hardware, and the "glue" logic that surrounds these devices. The "glue" chips include a MM74PC74 dual flip flop, three MM74PC04 hex inverters, six MM82PC08 transceivers, and three MM74PC138 3X8 decoders. The first step in reducing these functions to a custom or semicustom LSI chip is to estimate their equivalent gate complexity. Typically, two-input gates in CMOS can be put together in order to realize any complex Boolean function. Using the two-input gate as the equivalent gate, the complexity of the glue logic is shown in table V.

Table V. Equivalent Gate Count

Description	No. in Circuit	Equivalent Gate Count	Total for Device
MM74PC74	1	15	15
MM74PC04	3	4	12
MM82PC08	6	20	20
MM74PC138	3	23	69
Total for glue chips			216

Note that the 13 dual inline packages that comprise the glue chips can be replaced by a custom or semicustom chip that has at least 216 equivalent gate complexity. A

straight forward approach to designing a custom integrated circuit has been developed by Carver Mead at the California Institute of Technology and Lynn Conway at the Xerox Palo Alto Research Center.

The Mead-Conway Methodology

The Mead-Conway approach to integrated circuit design is a university-oriented system which implements a standard floorplan LSI design and is characterized by the use of regular structures, wiring by cell abutment, scalable design rules, simplified timing models, simple circuit primatives, and architecture and interconnect emphasis in the design cycle (23:222).

In 1981 over 60 universities taught a course using the Mead and Conway text (14). The approach is simplified and computer aided to the point that students can design, build, and test VLSI circuits within a semester. The student starts by defining the function of the complete system and partitioning the system into major functional modules. Next the student makes a floorplan by physically placing the modules in an arranagement which simplifies the signal flows. The modules are implemented using many replications of a few standard cells which are stored in a computer file. This technique increases the utility of computer aided design tools and removes most of the tedious design details from the student. A scalable set of design rules is used so

the student is not concerned with the process used during the design period. The student's design can be built in silicon using the MOS Implementation Service.

MOS Implementation Service (MOSIS)

The MOS Implementation Service (MOSIS) provides custom devices that are designed using the Mead-Conway methodology. MOSIS was developed by the Defense Advanced Research Projects Agency (DARPA) to provide fast fabrication at reasonable cost of MOS devices. In addition to DARPA, MOSIS is used by other research and development agencies and several universities.

The device processing is very simple for the user. The user, such as AFIT, stores the device design in a file which is compatable with MOSIS format. This file is transfered via the ARPANET to the MOSIS system where it is combined with many user's projects into one mask generator file. A wafer contains many projects, and the cost of each device type per wafer is a fraction of the processing cost. MOSIS acts as a broker, and hires an IC manufacturor to process the wafer and package each die in standard dual inline packages (DIPs). MOSIS reports the successful completion of more than 20 fabrication runs by various commercial vendors in a typical turn-around time of four to six weeks (4:25).

The recorder schematic shows several dozen miscellaneous chips in addition to the major components. These minor "glue" chips could be replaced by one custom MOSIS chip. NMOS technology devices are deliverable today

under MOSIS. All of the functions of the six MM82PC08 transceivers can be handled internally on the MOSIS chip. The approximate device count for such a chip is found in Table VI.

Table VI. Device Count in NMOS Technology

Device	Qty	Transistors per Device	Transistor Total
Inverter, simple	48	2	96
Inverter, super	100	4	400
NAND, two-input	3	3	9
NAND, Three-input	5	4	20
NAND, four-input	7	5	35
D flip flop with set and clear	2	25	50
Total Transistors			610

The transistor count for the MOSIS-produced chip indicates chip physical size and power requirements. The NMOS dice contain both depletion mode and enhancement mode MOSFET's (Figure 3). The NMOS MOSFETS are members of the family of devices which operate through the conduction of electrons but not holes; therefore, they are classed as unipolar. NMOS MOSFETS can be envisioned as a bar of doped silicon with source, drain, and gate areas. The source and drain regions are identical. Each is a shallow tub of silicon which is oppositely charged from the bulk silicon. The source and drain are close together physically, and the gap between them defines the gate region. All three regions have an electrical contact. An N-channel MOSFET has negatively doped drain and source and a positive gate. When a voltage is impressed from drain to source (or vice versa)

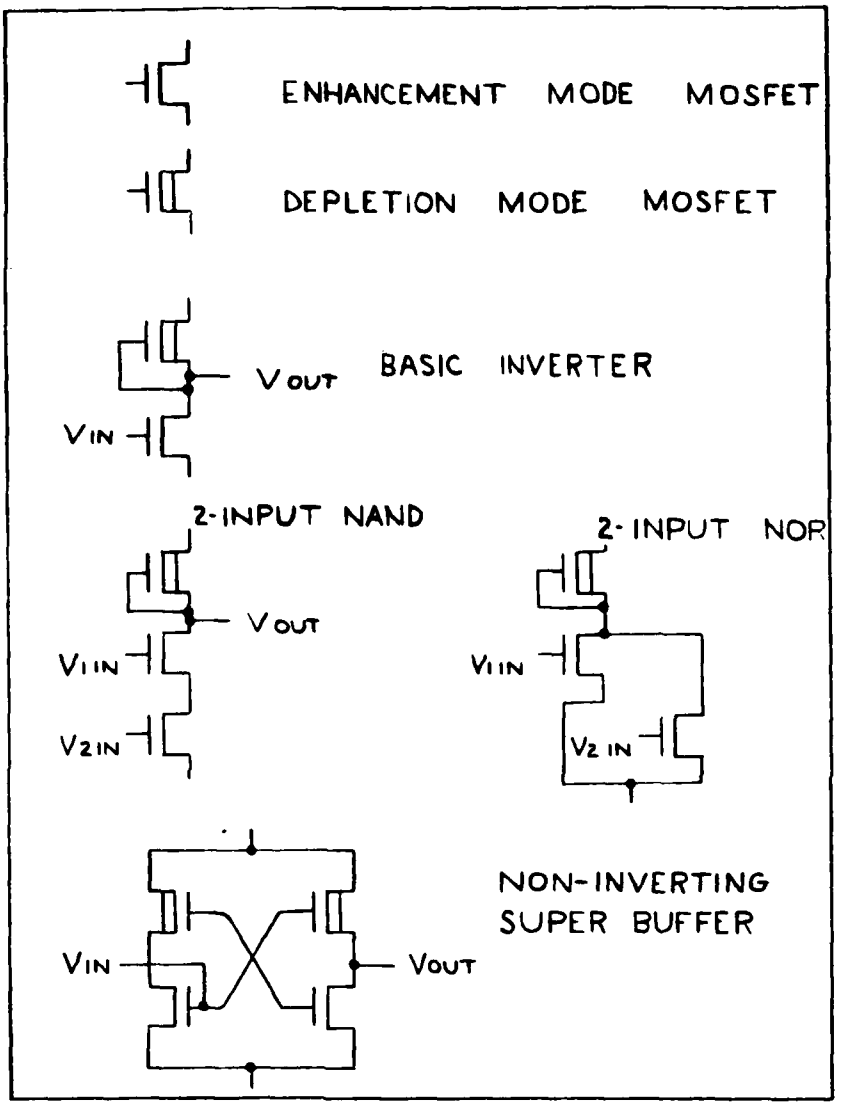


Figure 3. NMOS Gate Implementations

the flow of electrons is impeded by the positive gate region which lacks free electrons needed to support electron current flow. When the voltage on the gate is neutral, the device offers a high resistance. As the gate becomes positive, free electrons are attracted into the gate region and become available to carry current. The drain-to-source potential differential decreases. This transistor is an enhancement mode N-channel MOSFET.

The N-channel depletion mode MOSFET has strongly doped negative source and drain, and a narrow negative implanted region across the gate. The device will conduct current from drain to source when the gate voltage is neutral. As the gate voltage is lowered, electrons are forced away from the gate region and the source to drain current is deprived of them as charge carriers. Thus, the source to drain voltage rises (4:433-8). The logic gates in Figure 3 use transistors for loads because their small size and relatively simple processing allow more functions in a smaller space and at lower cost than resistive loads. The processing would be less complex if enhancement mode transistors were used for loads; however, the devices would have lower gain in the transition region and require a second power supply voltage (7:657,67).

A disadvantage of the MOSIS process for this thesis is the limited experience at this institution. No one here has used the MOSIS system, and the school will not have the software running to implement the Mead-Conway methodology until spring 1983. This date it too late to support the

hardware effort for this thesis. A disadvantage of NMOS is that it requires more power than a functionally equivalent CMOS circuit. MOSIS is developing a CMOS capability and future investigators may consider MOSIS-CMOS.

Semicustom Gate Universal Array (GUA)

AFIT has developed the PG system which produces a magnetic tape suitable to control a pattern generator. PG is a set of C-language computer programs written at AFIT by Major Harold Carter which compile the designer's decription of IC photolithographic layers, produce a magnetic tape of commands for a pattern generator, and offer other utilities to aid the designer (2). The PG system is documented by:

a. Users guide to the PG system;

b. Description of Series 2000 Electromask Pattern Generator

c. 3600 Pattern Generator Magtape Format;

d. C-language Pattern Generator Program, Main routine and Global Variables for the PG program;

e. C-language Lexical Analyzer for the PG Program;

f. C-language PG Program "pggrammer.c";

g. C-language PG Sort Program;

h. C-language PG Plot Program;

i. C-language PG Tape Utility;

j. and, C-language ESPLIT Utility Program.

Consequently, the designer can select a semicustom commercial product, layout the chip using manual methods, and reduce the layout to a magnetic tape. The tape can be

used by a contractor to generate masks and perform the final processing steps on the wafer. This wafer could be a GUA.

A GUA is an integrated circuit which implements complex Boolean logic functions by the repetitive use of a standard logic cell. The requirement often arises to build an electronic circuit which is modeled by a Boolean function. In an electronic implementation of a Boolean expression, a logic cell implements an operation. Electronic implementations which use a standard logic cell to implement unique functions are GUA's.

GUAs are referred to as "semicustom" integrated circuits because the basic device is identical for all users and consists of the repetitive reproduction of a standard logic cell. Only the final metal interconnect pattern is varied to produce a unique function. The GUA concept enables the manufacturer to produce standard devices in large quantities and take advantage of the economy of large volume production. Thus, the designer with a requirement for a small number of devices can implement the design on a semi-custom chip at less cost than a totally unique integrated circuit.

Typically, the unpackaged integrated circuit is made in one of the popular IC technologies and measures 0.25 inches square by 0.10 inch thick. Areas on the chip are reserved for logic cells, interconnect wiring, and I/O pads.

The logic cell areas are filled with the standard logic cells which are placed in repetitive ordered rows. The basic cell is an integrated circuit device which implements

a simple Boolean function. A common selection for a GUA logic cell is the two-input NAND gate which produces the negated "AND" operation.

The wiring channels contain aluminum lines that interconnect the cells with each other and with the I/O pads. The layout of these lines is made by the designer. This final layer of interconnecting lines makes a GUA unique for a given application.

The pad areas are along the periphery of the chip and are reserved for contact pads which are used to bond wires from the chip to the package. A pad is a square of aluminum, typically 0.003 inch on a side. The layout of the interconnecting aluminum lines is made by the purchaser, and given to the manufacturer as a specification when the purchase order is placed. The manufacturer processes the final metal layer on standard chips from stock.

The TCS-093 GUA

The TCS-093 family of GUAs built by RCA was seriously considered for the hardware for the recorder because TCS-series wafers are made available to AFIT along with a complete design package. The TCS-093 GUA is 0.240 inches square and contains a total of 632 cells, each cell contains two p-type and two n-type transistors (22).

The TCS-093 GUA has 64 pads located around its perimeter which can be used for connections to input and output pins. The assumption is made that all the glue gates on the schematic are implemented in the GUA. Transceiver U17 can be replaced by a simple buffer. If all these gates were replaced by a single GUA, the GUA would require the 106 pins for input and output. Figure 4 and Table VII shows how this number is derrived.

The table shows that the GUA approach would require more than one device package. Since the expense in a GUA is involved in the design, and a single wafer processing results in dozens of devices, the logical approach is to try to use multiple copies of an identical GUA design to satisfy the circuit function.

The packages to be replaced by GUAs are seven MM82PC08 three MM74PC138 3X8 decoders, twenty inverters three two-input NOR gates, and two two-input NAND gates. Figure 5 pictorially shows how this could be done in a three chip implementation, and Table VIII shows the pin count for this layout. Each TCS-093 die is identical, but three identical dice would be used to replace the glue chips.

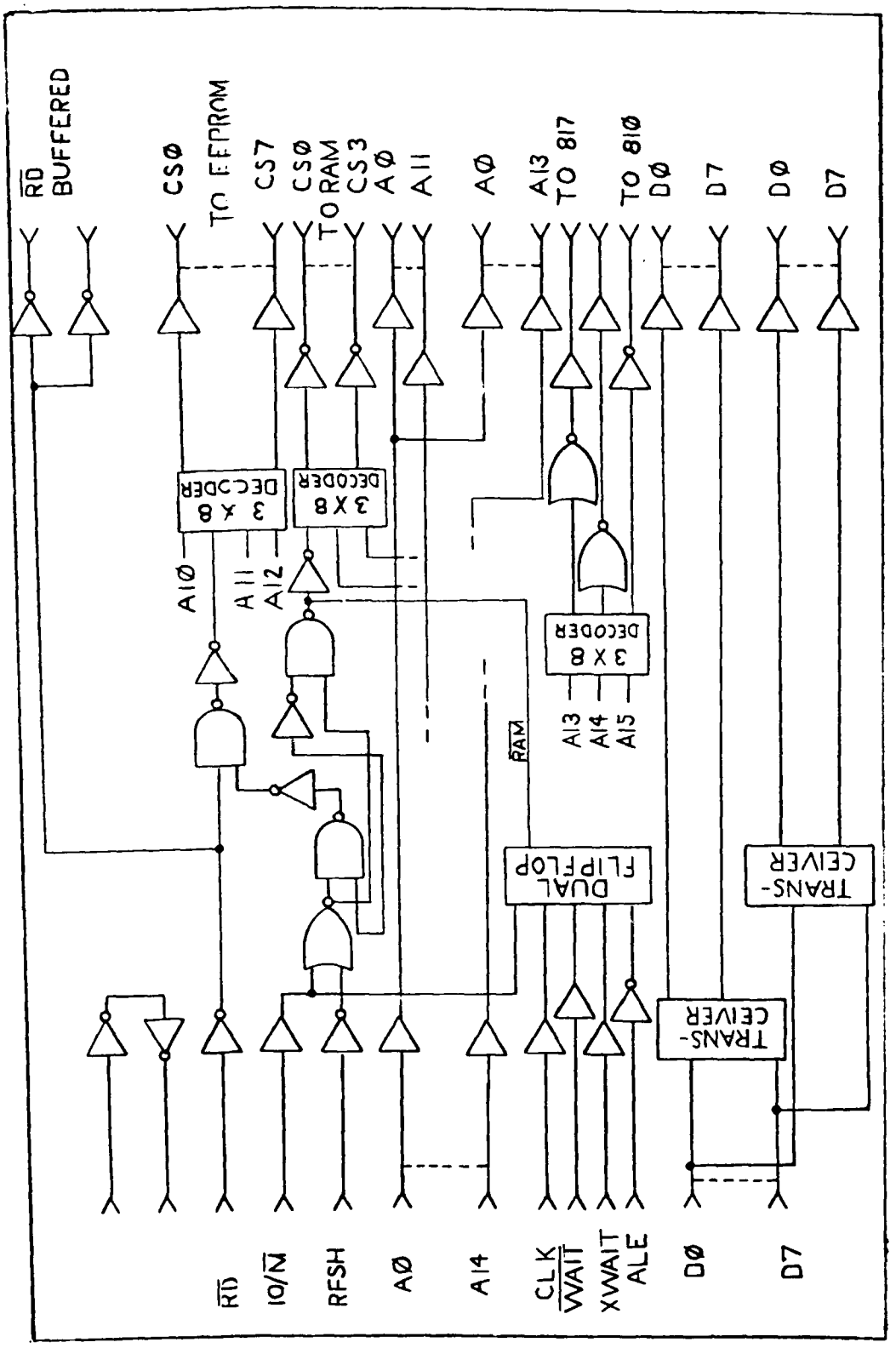


Figure 4. Single TCS-093 GUA Implementation Schematic

Table VII. GUA Pin Count

Function	Pins Required
IO/M*	1
RFSH*	1
A0-A15 IN	16
D0-D7 IN	8
+5vdc	1
GND	1
RD*	1
D0-D7 to EEPROM	8
A0-A13 to EEPROM	14
RD* out	3
WR* in	1
WR* out to RAM	1
A0-A10 to RAM	11
D0-D7 to RAM	8
CE1* to ADC 0817	1
Tri-state to ADC0817	1
START to ADC0817	1
REF OUT to ADC0817	1
RSTC in from ADC0817	1
RSTC* TO NSC800	1
CS0-CS7 to EEPROM	8
CS0-3 to RAM	4
D0-D7 TO 7220	8
CLK IN to 7220	1
CLK OUT to 7220	1
WR* to 7220	1
CS to 7220	1
A0 to 7220	1
Total Pin Count	106

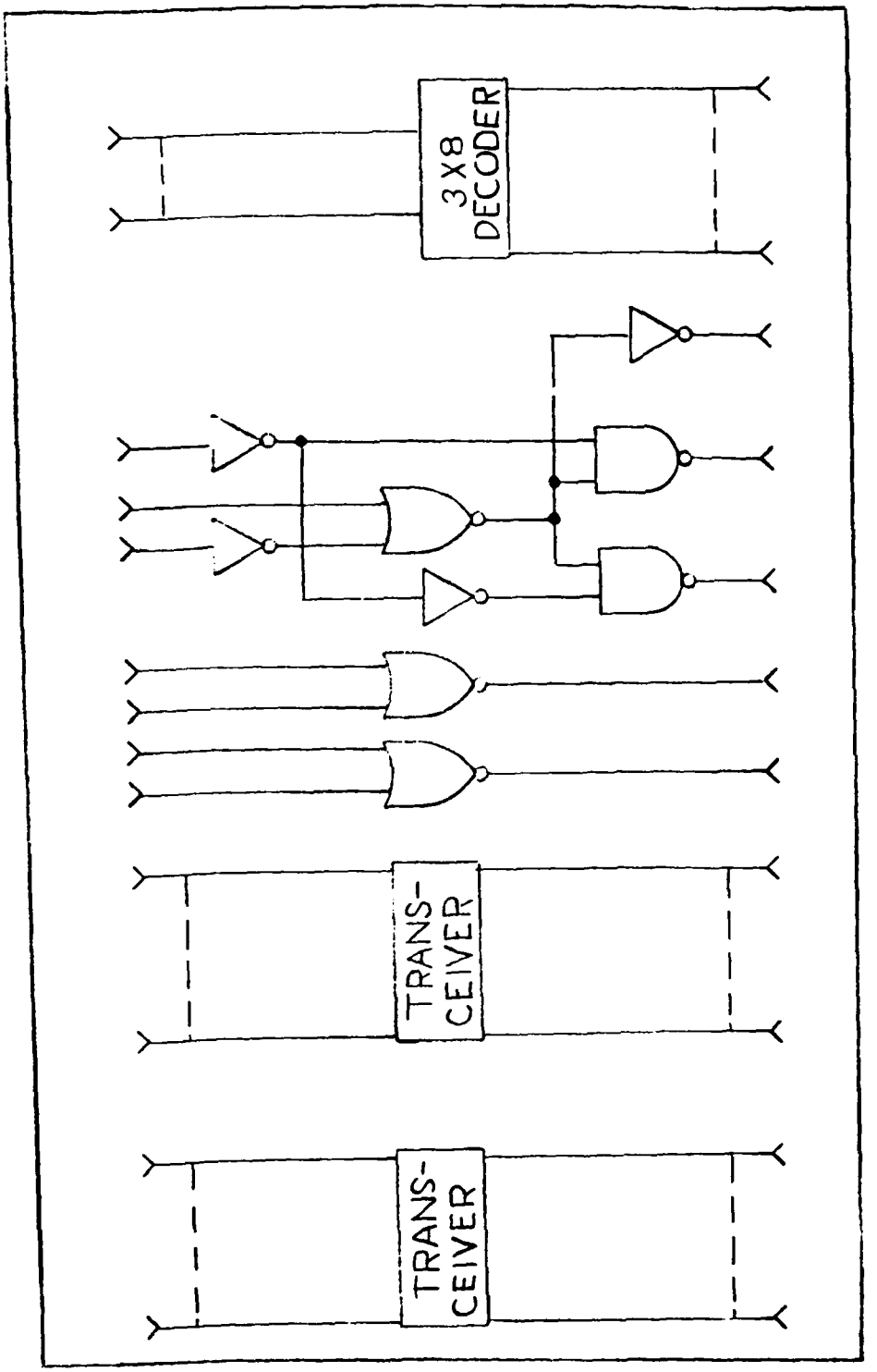


Figure 5. Triple TCS-093 GUA Implementation, Logic on Each Die

Table VIII. Proposed GUA Pin Count

Function	Quantity of Pins
input signals ,transceivers	16
output signals, transceivers	16
enable signals, transceivers	2
select signals, transceivers	2
input signals, decoders	3
select signals, decoders	3
enable signals, decoders	3
output signals, decoders	8
+5vdc and grd	2
glue logic	12
Total Pin Count	64

The pin count rests at 64 which is the absolute maximum supported by the TCS-093. A casual inspection of the pin count may indicate that room for growth doesn't exist, and good design practice allows room for growth. A deeper examination shows that Table VIII reserves 16 pins for transceiver outputs, five pins for chip enables, and five pins for chip selects. The 16 pins for transceiver inputs can be reduced to eight by designing on-chip logic which insures that one transceiver is tri-stated at all times that the other is active. Further, on-chip decode logic can be built to reduce the wires required for chip selects and chip enables.

Designing a GUA for the recorder does pose practical problems. The first problem is time. A team which included the author has layed out a TCS-093 GUA using the PG system and the effort required approximately one man-year of effort. Assuming an optimistic schedule and learning curve, this thesis may complete the GUA in three months. The large effort devoted to the GUA would deprive this thesis of the effort to design, build, and test the bulk of the recorder design.

Programmable Array Logic Device (PAL)

Programmable Array Logic devices are available which can be programmed by the user to implement a Boolean function. Typically, five to 12 standard SSI and MSI functions can be implemented on a single PAL (28:238). Many PALs have a complexity of near two hundred equivalent gates which compares nicely with the recorder equivalent gate count reported in Table V; however, PAL designs may allow for eight or ten outputs. This is low for the recorder requirements. Table IX is a survey of available TTL PALs and their characteristics which are germane to this discussion. No CMOS PALs have been identified as being commercially available. The limit on tri-state output means that one PAL would be required for each MM82PC08 transceiver.

Table IX. Typical TTL PALs

Part Type	Array Inputs	Output Registers Tri-state Buffers	Gate Equivalent
PAL 16L8	16	8	368
PAL 16R4	16	4	400
PAL 16R6	16	6	410
PAL 16R8	16	8	424
PAL 20LR	20	8	376
PAL 20R4	20	4	400
PAL 20R6	20	6	410
PAL 20R8	20	8	424
FPLA 16X48X8	16	8	380
FPLS 16X48X8	16	8	540
FPLA 18X32X10	18	10	318
FPLS 16X32X12	16	12	456

It is concluded that the thirteen devices which comprise the glue logic in the recorder can be implemented in six PALs; however, the available TTL devices are not suitable because of their power consumption (10:327-341).

Leadless Chip Carriers

A Hughes HNVM 3008 EEPROM die measures 0.214 inch by 0.190 inch, but the standard 24-pin dual inline package (DIP) that it is supplied with measures 1.310 inch by 0.6 inch (27:4-7). Thus, the DIP covers 19 times more board area than the die. Any package technique that improves on this ratio is attractive, and leadless chip carriers mounted on the board surface is one such improvement.

The leadless chip carrier (LCC) is essentially the central portion of a DIP with the pins and end portions removed so that the squared center portion remains. The leads are replaced by contact pads.

The square LCC is made of ceramic similar to ceramic DIP material. LCC sizes have been standardized for military applications, and range in size from 16 to 84 pins (8:152). The CMOS devices selected for the recorder will be available in LCC because of the weight, volume, and reliability advantages of LCCs. It has been forcast that by 1990 approximately 36 percent of the worldwide IC packages will be LCC (12:3).

A recorder design employing leadless chip carriers mounted on a circuit board is attractive; however, devices in LCC will not be available in time to use with this thesis (3:192). *Future investigators should consider this* approach.

Dual Inline Packages

Dual Inline Packages (DIPs) are widely used today becuase DIPs represent a cheap, proven technology. DIPs consist of a die mounted on a frame with leads. The frame and die are encapsulated in plastic or sealed between ceramic layers to provide mechanical integrity. The leads are arranged in two parallel rows. The spacing between pins is 0.1 inch and the spacing between the parallel rows is 0.3 inch for DIPs with 20 or fewer leads and 0.6 inch for larger DIPs (27:4-3-8).

All CMOS devices in the recorder design are manufactured in DIP and are stocked by local suppliers. The recorder design could be built around DIPs if they can be packaged into the available space. The overall recorder dimensions are specified to be less than 2 X 5 X 9 inches which must include the MBM board which requires a volume of approximately 1 X 4 X 4.5 inches. Assuming that the battery will be packaged separately, then a straight forward design would include all remaining electronic parts on a board which requires a maximum volume of 1 X 5 X 9 inches. Hand calculations and sketches disclosed that this could be done using a four layer printed circuit board (PCB). Arrangements were made with the AF Avionics Laboratory to provide facilities for the computer aided design and fabrication of a PCB.

Computer Aided Design of Printed Circuit Boards

Computers are useful in the physical design of printed circuit boards. In general, computer aided design (CAD) of printed circuit boards may include any of the functions of synthesis, partitioning, component placement, wire routing, analysis, simulation, and testing. The trend today is toward more CAD help, but the state of the art assigns the computer to calculations and repetative tasks, and relies on the human designer for pattern recognition and judgement. For the purpose of this thesis, CAD was restricted to wire routing.

Hardware and Software

Software for the CAD system used for this thesis consisted of the Applicon 870 Graphic Operating System (AGS), the Digital Equipment Corporation Disk Operating System (DOS), and the Applicon Routing Package Release 1.1. Hardware used for the CAD included a PDP-11 minicomputer, a disk drive, tape deck, graphics display CRT, teleprinter, and input tablet with pen and a graphics keyboard. CAD is a problem solving process that requires creating the circuit board pictorial, generating a wiring netlist which describes how the pictorial components are electrically interconnected, routing the printed circuit board, and editing the printed circuit board.

Creating the Pictorial

Definition of the physical dimensions of the PCB and its components is essential. First, the CAD operator defines the overall board dimensions of the graphics CRT using the input tablet and pen and the graphics keyboard. Next, the operator creates a component on the board. This component is stored in a computer file which can be used to reposition, rotate, or replicate the component. In this manner, the complete board pictorial can be defined. The final pictorial for the recorder microprocessor board is shown in Figure 6.

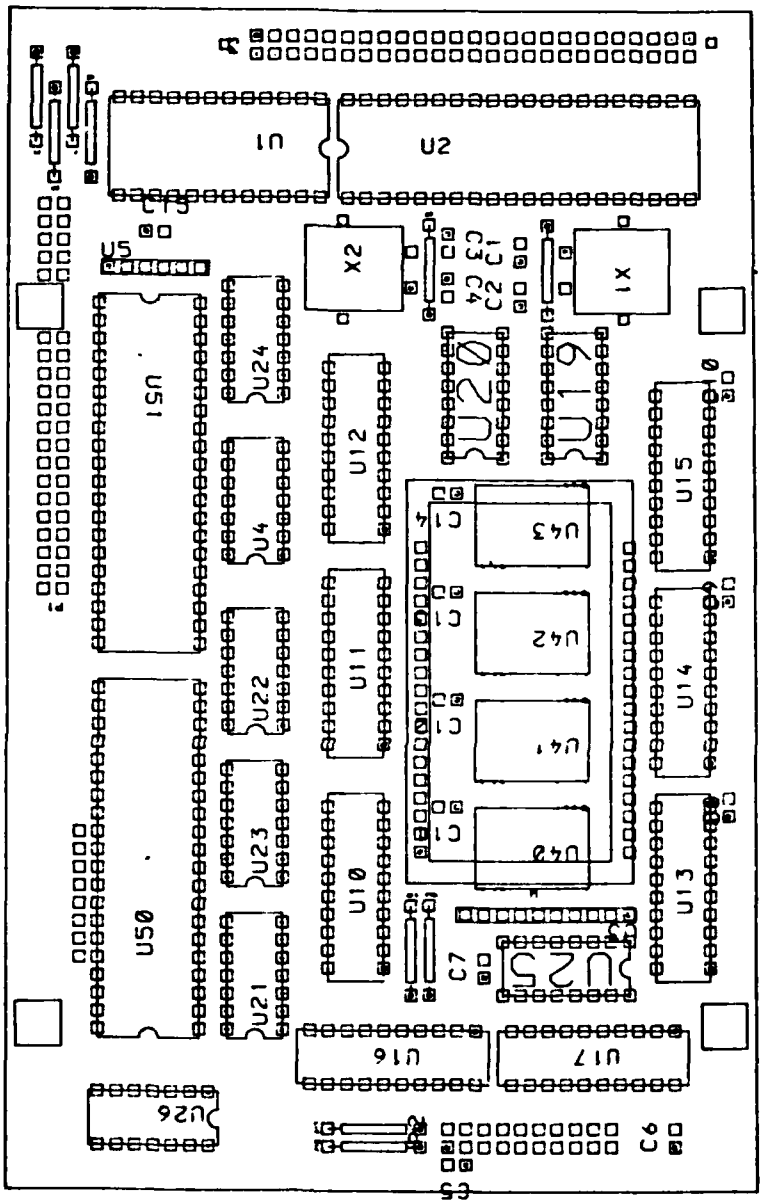


Figure 6. Flight Recorder Microprocessor Board Pictorial

Wiring Netlist

Each component on the board is uniquely named and its pins are numbered. The designer enters an exhaustive list of the electrical connections among all the pins. The final wiring netlist for the recorder is shown in Figure 7.

Routing

The wiring netlist is merged with the pictorial file and the software attempts to determine a routing pattern on one side of the board which will satisfy the wiring netlist. When the route becomes blocked, the software plans on a conductive hole through the board (via). The software attempts to complete the wire on the second side.

The CAD procedure has only been partially successful in routing the board because computer speed and the algorithm design have placed practical limits on the routing attempt. The first attempt at routing the recorder board in two layers produced the statistics found in table X.

Table X. First Routing Statistics

Number of Pins	=	748
Number of Vias	=	418
Total Wires	=	506
Total Connected Wires	=	267
Percent Total Wires Completed	=	52.77%

The board designer and the CAD operator reviewed the results and decided to make changes and rerun the routing program. First, it was clear that some of the wiring

```
 TY BUBBLE
U1   24   U1   11   U1   14   U2   40   U3   01   U4   14   U4   13   U10  20
U11  11   U11  20   U12  11   U12  20   U13  20   U14  11   U14  20   U15  11
U15  20   U16  20   U17  11   U17  20   U19  06   U19  16   U20  06   U20  16
U21  14   U22  14   U23  14   U24  14   U25  16   U26  14   U50  07   U50  40
U51  17   U51  37   U51  19   P1   26   P1   13   P2   01   D1   01   C6   02
C7   02   C8   02   C9   02   C10  02   C5   02   A3   02   U5   01   A12  02
A13  02   A14  02   A15  02   *
U1   01   U1   12   U2   20   U4   07   U10  10   U11  10   U12  05   U12  06
U12  14   U12  15   U12  10   U13  10   U14  10   U15  04   U15  05   U15  07
U15  08   U15  10   U16  10   U17  10   U17  09   U17  03   U17  02   U17  01
U19  08   U19  05   U20  03   U20  05   U20  08   U21  07   U22  07   U23  07
U24  07   U25  04   U25  05   U25  08   U26  07   U50  01   U50  20   U51  20
U51  23   M    01   P1   01   P2   02   C1   02   C2   02   C3   01   C4   02
P1   20   C6   01   C7   01   C8   01   C9   01   C10  01   C15  01   C5   01
*
U1   15   U11  01   U14  01   *
U1   17   U11  02   U14  02   *
U1   19   U11  03   U14  03   *
U1   21   U11  04   U14  04   *
U1   04   U11  05   U14  05   *
U1   06   U11  06   U14  06   *
U1   08   U11  07   U14  07   *
U1   10   U11  08   U14  08   *
U2   01   U51  36   U12  01   U17  07   U15  01   *
U2   02   U12  02   U51  35   U15  02   *
U2   03   U19  01   U51  34   U15  03   *
U2   04   U12  03   U51  33   *
U2   05   U12  04   *
U2   06   U21  03   U25  01   *
U2   07   U25  02   *
U2   08   U25  03   *
U2   12   U10  01   U51  24   U50  12   U1   16   U16  01   U13  01   *
U2   13   U10  02   U51  25   U50  13   U1   18   U16  02   U13  02   *
U2   14   U10  03   U51  26   U50  14   U1   20   U16  03   U13  03   *
U2   15   U10  04   U51  27   U50  15   U1   22   U16  04   U13  04   *
U2   16   U10  05   U51  28   U50  16   U1   03   U16  05   U13  05   *
U2   17   U10  06   U51  29   U50  17   U1   05   U16  06   U13  06   *
U2   18   U10  07   U51  30   U50  18   U1   07   U16  07   U13  07   *
U2   19   U10  08   U51  31   U50  19   U1   09   U16  08   U13  08   *
U2   09   U50  02   U50  03   U4   03   *
U2   21   U5   02   *
U2   22   U50  06   *
U2   23   U26  10   *
U2   24   U24  06   *
U2   25   U26  12   *
U2   28   U21  05   *
U2   30   U24  01   U1   13   U50  11   *
U2   31   U15  06   U50  10   U17  06   U23  12   *
U2   32   U12  07   U50  09   U12  08   U17  05   U23  08   U16  11   *
U2   33   U24  10   A2   01   *
U2   34   U4   12   U23  03   U25  06   *
U2   35   U1   02   *
U2   36   U5   03   P3   47   *
U2   37   U50  04   P3   41   U26  09   *
U2   38   P3   42   U4   10   U4   05   *
U2   39   U5   04   *
U4   0.   U4   02   *
U4   01   U5   05   *
U4   04   U22  11   U20  04   U13  09   U14  09   U15  09   *
U2   11   X1   01   A8   01   C1   01   *
U2   10   X1   02   A8   02   C2   01   *
C15  02   A1   01   A3   01   D1   02   *
A1   02   A2   02   U24  13   *
U24  11   U24  12   *
```

Figure 7.
Flight Recorder Microprocessor Board Wiring Netlist,
Sheet 1 of 3

```
U15  14   A15  01   *
U50  05   U51  22   *
U50  08   U24  08   *
U50  21   P1   03   *
U50  22   P1   04   *
U50  23   P1   05   *
U50  24   P1   06   *
U50  25   P1   24   *
U50  26   P1   23   *
U50  27   P1   22   *
U50  28   P1   21   *
U50  37   P1   07   *
U50  38   P1   25   *
U50  39   P1   02   *
U51  21   U23  10   *
U51  38   P1   27   *
U51  39   P1   35   *
U51  40   P1   28   *
U51  01   P1   36   *
U51  02   P1   29   *
U51  03   P1   37   *
U51  04   P1   30   *
U51  05   P1   38   *
U51  06   P1   31   *
U51  07   P1   39   *
U51  08   P1   32   *
U51  09   P1   40   *
U51  10   P1   33   *
U51  11   P1   12   *
U51  12   P1   34   *
U51  13   U24  05   *
U51  14   P1   11   *
U51  15   U51  18   *
U51  16   U51  32   U23  13   *
P2   20   U26  13   A13  01   *
P2   04   U26  11   A12  01   *
P2   05   U26  08   *
U17  16   P2   06   *
U17  15   P2   07   *
U17  14   P2   08   *
U17  13   P2   09   *
U17  12   P2   10   *
U16  19   P2   12   U3   03   *
P2   11   U3   02   *
U16  18   P2   13   U3   04   *
U16  17   P2   14   U3   05   *
U16  16   P2   15   U3   06   *
U16  15   P2   16   U3   07   *
U16  14   P2   17   U3   08   *
U16  13   P2   18   U3   09   *
U16  12   P2   19   U3   10   *
M    29   P1   14   *
```

Figure 7.
Flight Recorder Microprocessor Board Wiring Netlist,
Sheet 2 of 3

```
U26  02   A9   02   X2   02   C3   02   U17  04   *
U26  01   A9   01   X2   01   C4   01   *
A14  01   U12  13   M    20   *
U12  12   U13  11   U10  11   *
U19  02   U12  17   U20  01   *
U19  03   U12  16   U20  02   *
U12  09   U21  08   *
U21  09   U22  02   U23  01   U22  12   *
U21  04   U22  01   U21  01   *
U21  02   U22  13   *
U22  03   U10  09   U11  09   U19  04   *
U21  06   U23  02   *
M    03   U10  19   *
M    04   U10  17   *
M    05   U10  16   *
M    06   U10  15   *
M    07   U10  14   *
M    08   U10  13   *
M    09   U10  12   *
M    10   U11  19   *
M    11   U11  18   *
M    12   U11  17   *
M    13   U11  16   *
M    14   U11  15   *
M    15   U11  14   *
M    16   U11  13   *
M    17   U11  12   *
M    18   U12  19   *
M    19   U12  18   *
M    21   U19  07   *
M    22   U19  09   *
M    23   U19  10   *
M    24   U19  11   *
M    25   U19  12   *
M    26   U19  13   *
M    27   U19  14   *
M    28   U19  15   *
U25  14   U24  09   *
U25  13   U23  09   U23  11   *
U25  11   U17  08   U16  09   *
M    30   P1   08   *
M    31   P1   09   *
M    32   P1   10   *
```

Figure 7.
Flight Recorder Microprocessor Board Wiring Netlist
Sheet 3 of 3

completed by the machine was not accomplished as the designer had intended. Investigation disclosed that syntax rules for the wiring list had been violated during keyboard entry, and the list was corrected. Next, is was observed that P3 could be easily wired by hand in layers three and four and its connections were removed from the wiring netlist. It was hoped that removing this wiring would raise the percentage of total wires completed during the second run. Further, it was observed that board wiring could be simplified if very thin wires were threaded between each pair of pins on U40, U41, U42, and U43. The space between these pins is 30 mils across, thus 10 mil wires could pass between them with 10 mils clearance. Since the automatic router describes a standard 20-mil wire, it was decided to delete these parts from the wiring netlist and manually add these wires. Capacitors C11, C12, C13, and C14 are closely associated with U40-U43, and they were deleted from the wiring netlist, too. Finally, the board was obviously congested and the designer reviewed the product specification with a view to enlarging the board dimensions. The board was then enlarged from 4 inches by 6 inches to 4.10 inches by 6.60 inches.

The second routing attempt was completed with the results listed in table XI.

Table XI. Second Routing Statistics

Number of Pins	=	748
Number of Vias	=	361
Total Wires	=	349
Total Connected Wires	=	239
Percent of Total Wires Complete	=	68.48%

Examination of the route two results disclosed a significant number of incomplete wires that should run from the center of the board in the area of U51 and P1 to the bottom of the board in the area of U13, U14, and U15. Further, C5 could not perform its function in its present physical location. The components X1, A8, C1, and C2 were rearranged in a cluster near the position that they occupied for route two. Component U1 was moved to the side of U2. Route three was performed with the results found in Table XII.

Table XII. Third Routing Statistics

Number of Pins	=	748
Number of Vias	=	320
Total Wires	=	349
Total Connected Wires	=	220
Percent of Total Wires Complete	=	63.04%

Inspection of the route three results shows that the percent of wires complete is lower that route two. Investigation revealed that the more "efficient" layout of route three caused even more bunching of wires in the center area of the board, and removed wires from the less crowded corners. The net result was fewer completed wires.

The results of route three were discarded and the file of route two was retrieved for further work. It was quickly discovered that the software had again failed to interpret the wiring netlist as the designer had intended. The wiring netlist ends each wire with a star (*); however, the machine

interprets each empty field in the line as an end of wire indication. For example, the ground wire uses ten lines on the wiring netlist because it connects many circuit points. Each of these lines contains seven or less connections, but the line contains fields for eight connections. The software interpreted the ground wire as ten seperate wires. The documentation for the netlist did not state that vacant fields would be interpreted as end of wire marks. The wire netlist was corrected, and route four was run. Route four became the most successful attempted with 74 percent of the wires completely connected on two layers (Table XIII).

Each of the remaining connections were designed manually by an iterative process which consisted of completing a wire and then often repositioning it to facilitate the completion of another. The two layers which had been machine routed were modified during this manual process. In addition, layers three and four were designed.

Table XIII. Fourth Routing Statistics

Number of Pins	=	748
Number of Vias	=	329
Total Wires	=	349
Total Connected Wires	=	258
Percent of Total Wires Completed	=	74.04

It was recognized that the design process was prone to introduce errors and the wiring was checked exhaustively for mistakes. Checking was done by a yellow-line method. The method required large pen and ink plots of each PCB wiring

layer and a copy of the complete schematic. The plots were roughly five times scale, and a portion of one is displayed as Figure 8. Each connection was lined out with a yellow marker on the schematic and then the corresponding wiring path on the plots were lined out. Each error was noted as it was identified. At the end of the check, any unlined paths on the schematic or plots were rationalized. Over two dozen errors were identified during the first yellow line check. Corrections were made, and three errors were identified during the second yellow line check. One error was a previously identified one which had been improperly corrected, but the other two errors had not been discovered before. No errors were disclosed by the third yellow line check and the files were used to generate PCB artwork. The artwork is shown in Figure 9.

Selection of RAM

In order to minimize the overall dimensions of the recorder board, it was necessary to raise the memory density in the RAM and ROM area of the board. The Hitachi HM6116 RAMs are available in a 24-lead flat pack. These were planned because of their small physical size and availability.

A Hybrid EEPROM Package

The Hughes HNVM 3008 EEPROMs are available in die form and it was decided to mount these in a hybrid package that would resemble a DIP. The hybrid DIP would plug into the board and rest on top of the low-profile RAM flat packs.

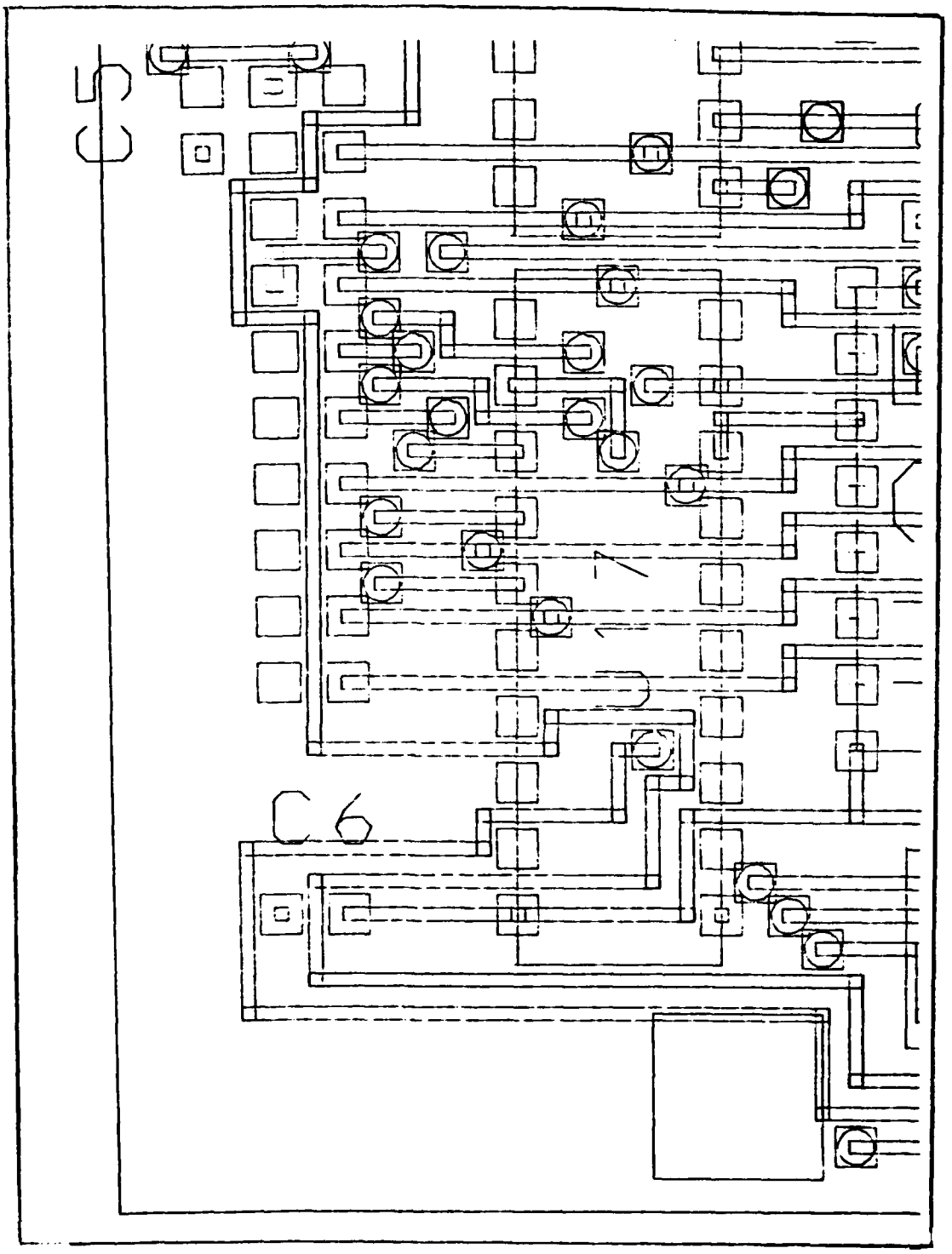


Figure 8. Portion of Microprocessor Board CAD Plot

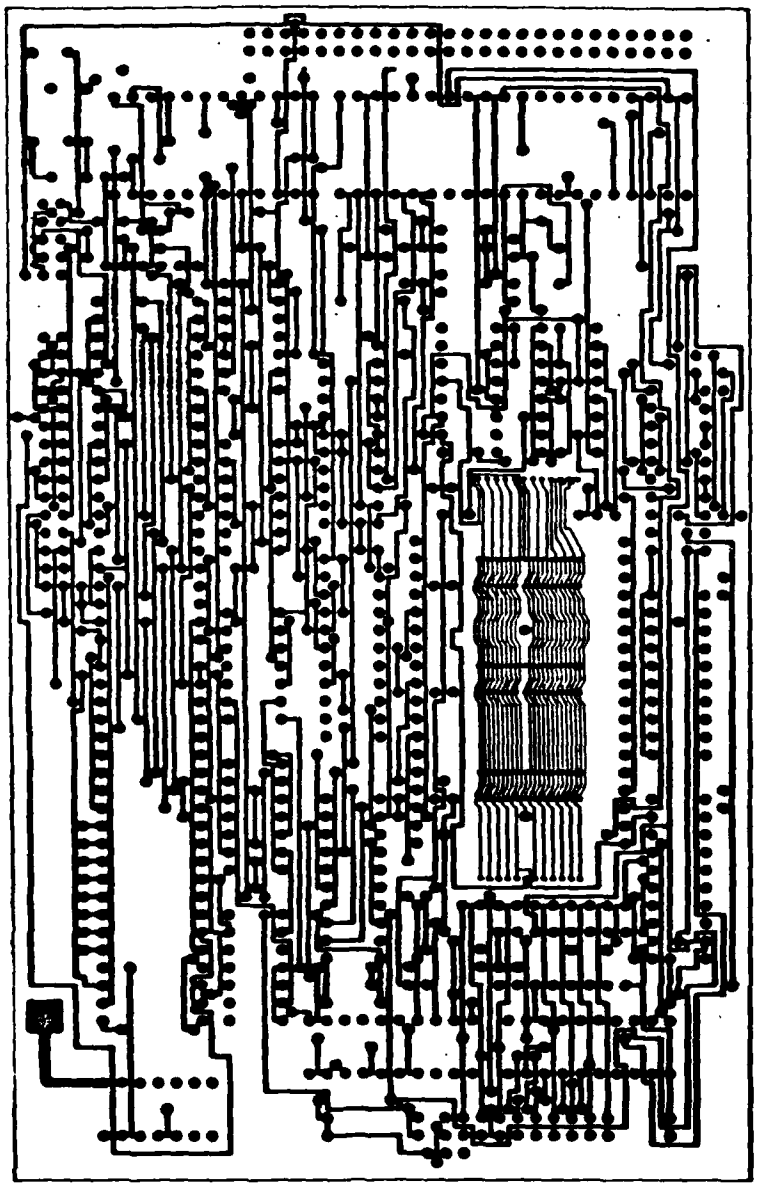


Figure 9.
Flight Recorder Microprocessor Board Artwork,
Sheet 1 of 4

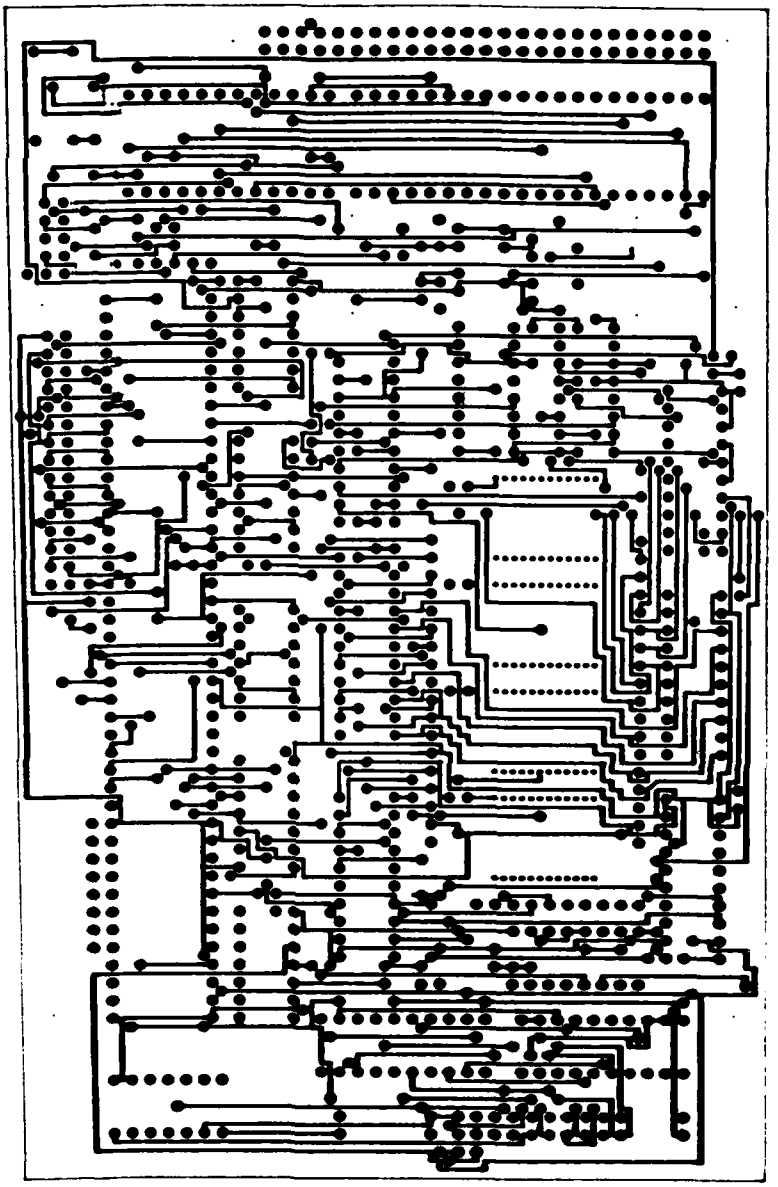


Figure 9.
Flight Recorder Microprocessor Board Artwork,
Sheet 2 of 4

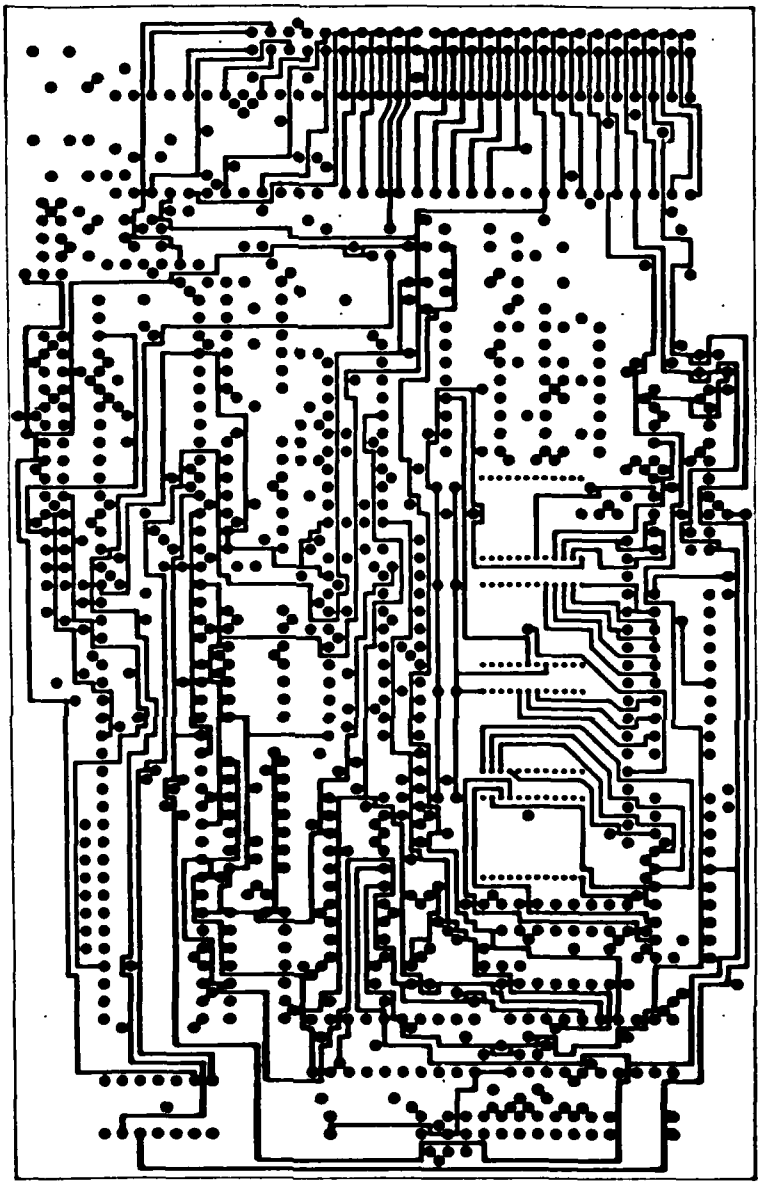


Figure 9.
Flight Recorder Microprocessor Board Artwork,
Sheet 3 of 4

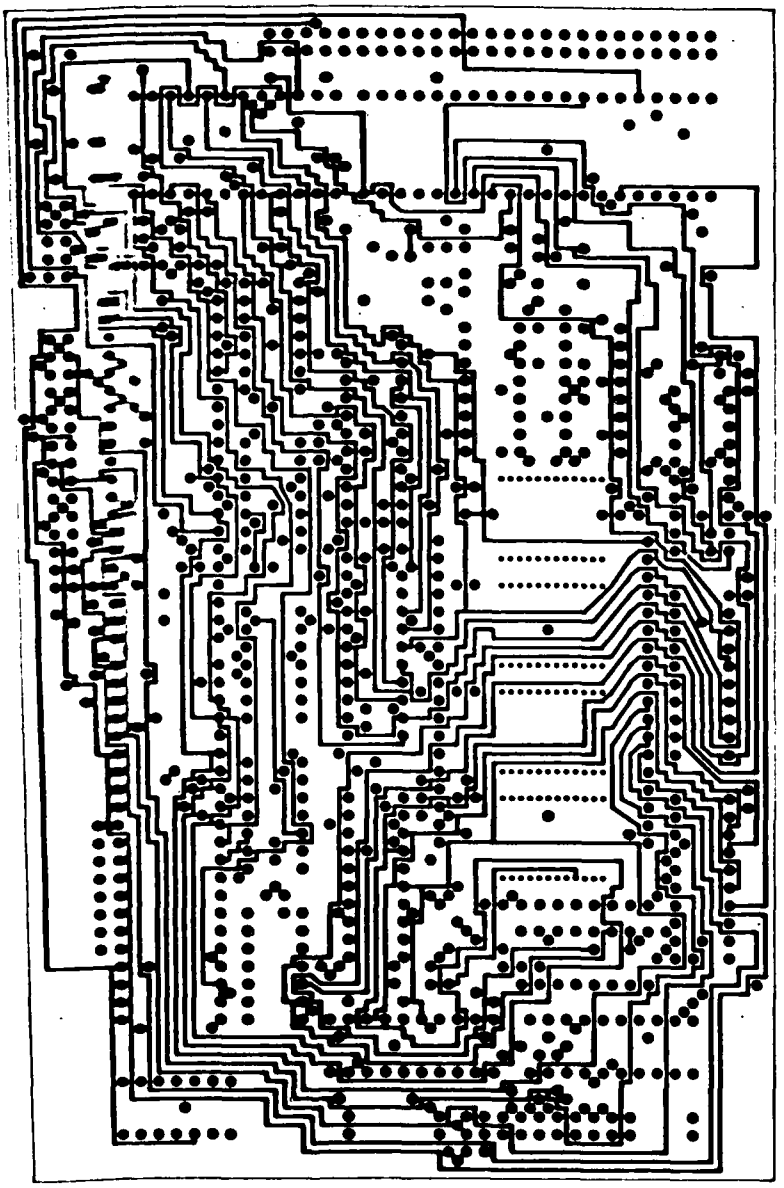


Figure 9.
Flight Recorder Microprocessor Board Artwork,
Sheet 4 of 4

The Hughes HNVM 3008 dice were not ordered at this time because the minimum quantity bid was 36 for a total cost which exceeded $2,400. For the present, it was decided to produce a test EEPROM module employing DIPs. This test module satisfied all functional requirements except volume, and it is satisfactory for all developmental testing. The test module schematic is shown in Figure 10.

Batteries

The recorder design is easily partitioned into three main parts; (1) the bubble memory board, (2) the microprocessor board, and (3) the battery pack. Discussion of the bubble memory board was quickly dispatched by the decision to buy a commercial product. The microprocessor board was discussed extensively, and its design became a major portion of the thesis effort. The third partition of the recorder is the battery pack.

Requirement. Measurements on the wire wrapped breadboard show that the recorder requires 160 milliamps at five volts to power the microprocessor board, and 90 milliamps to power the bubble memory board. The total five volt requirement is then 250 milliamps. In addition, the bubble memory board requires 160 milliamps at 12 volts for periods when the bubbles are being read or written and 20 milliamps when the bubbles are quiet. A typical duty cycle may read or write to the bubbles 25 percent of the time. A 7110 bubble can be completely dumped in about two seconds. In addition to power, safety is an important consideration in battery selection.

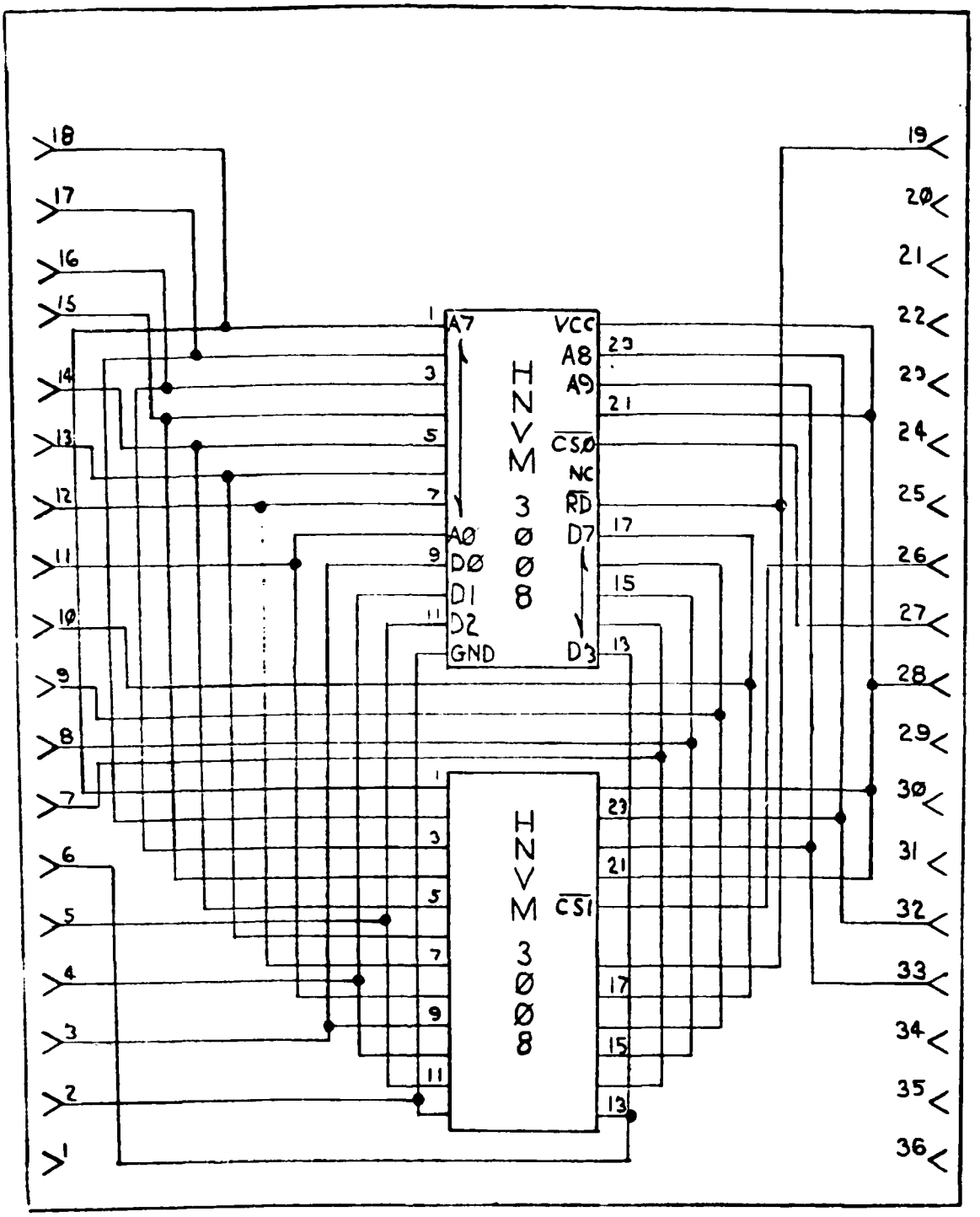


Figure 10. EEPROM Test Module Schematic

Safety. Various batteries exude explosive gas, contain caustic liquids, or explode with misuse. A safe battery is obviously very important for man portable equipment. Safety has additional considerations for a battery which is attached to an aircrew member who is operating a high performance aircraft. In addition to sea level hazards, the recorder battery may experience rapid changes in ambient pressure.

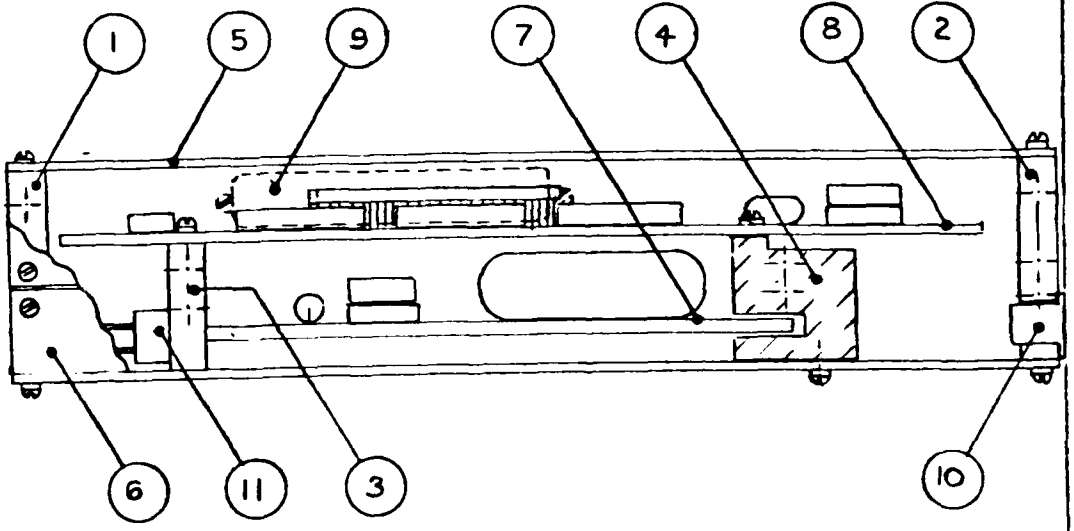
Physical Design. In that a battery is two or more series or parallel-connected galvanic cells (1:264), the recorder power pack constitutes a battery. The recorder battery supplies both five and twelve volts.

The battery pack is housed separately from the bubble and microprocessor boards and consists of a case, individual cells, and a connecting cable. The separate housing concept allows the weight and volume of the recorder to be distributed on the host for comfort. Further, the simple plug interface allows the battery design to be modified without any change to the rest of the recorder.

Nickel-cadmium battery cells were selected because they have been used in similar equipment without a safety consequence. Further, nickel-cadmium cells have good temperature and shock characteristics, a flat voltage discharge curve, and excellent recharge cycle life (1:264-8).

This chapter has delt with many technologies which may be appropriate to build into the flight recorder. These past pages have explained how and why the recorder has been

partitioned into three main subassemblies; (1) the battery pack, (2) the magnetic bubble memory board, and (3) the CMOS microprocessor board. The flight recorder mechanical drawings are shown in Figure 11. Finally, this chapter has described how the three subassemblies are designed. Yet the design process does not end with the design, and the next chapter develops an evaluation program designed to feed back improvements into the product before it is placed into its intended service use.



11	CONNECTOR, TRW CINCH NO. 251-22-30-160
10	POWER PLUG, AMPHENOL NO. 223-1505
9	SENSOR PLUG, CINCH NO. DD50
8	MICROPROCESSOR BOARD
7	MAGNETIC BUBBLE BOARD
6	BOTTOM SHELL
5	TOP SHELL
4	RIGHT SUPPORT
3	LEFT SUPPORT
2	RIGHT END PLATE
1	LEFT END PLATE

ASSEMBLY DRAWING

Figure 11. Flight Recorder Mechanical Drawings, Sheet 1 of 6

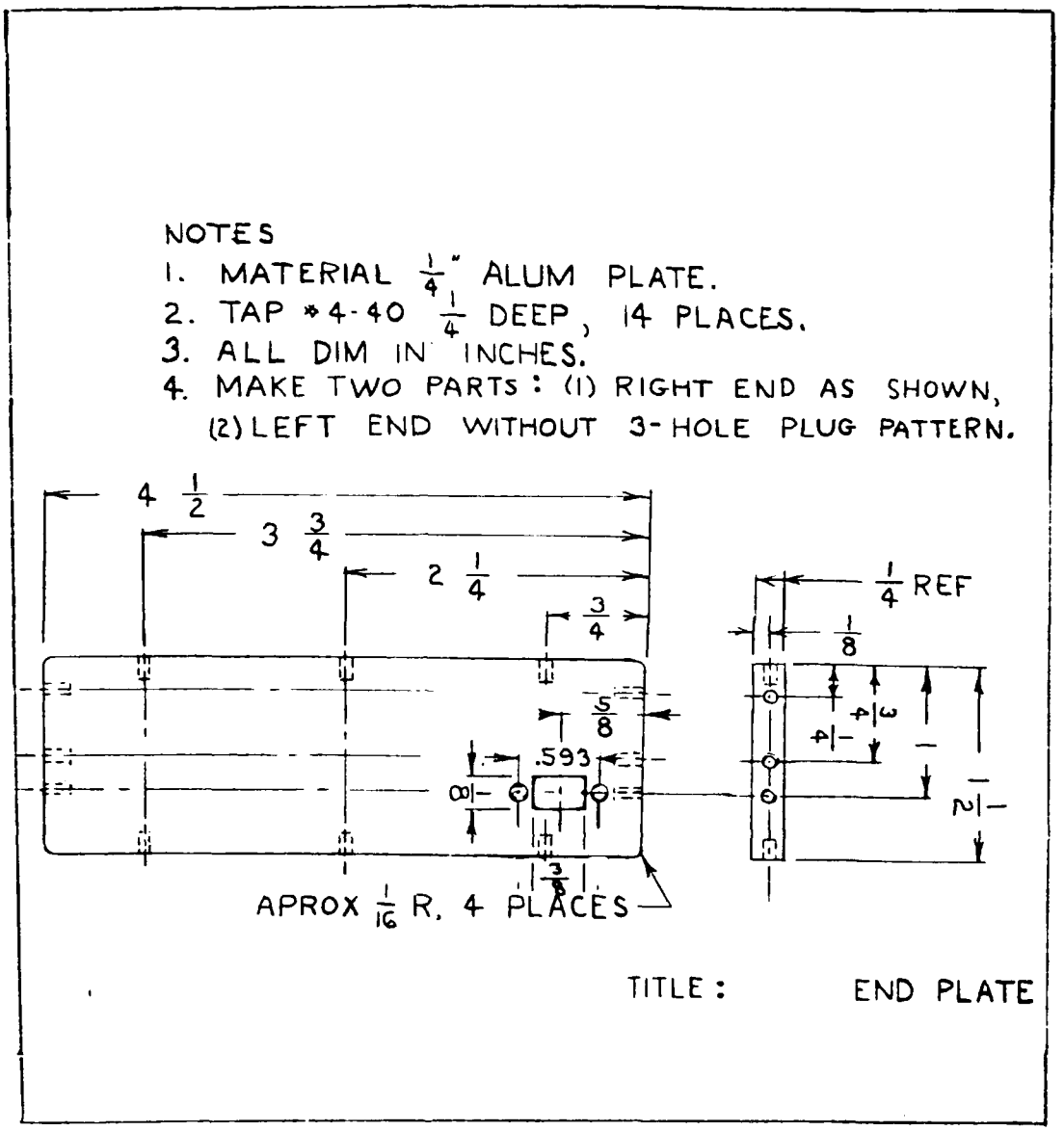


Figure 11. Flight Recorder Mechanical Drawings, Sheet 2 of 6

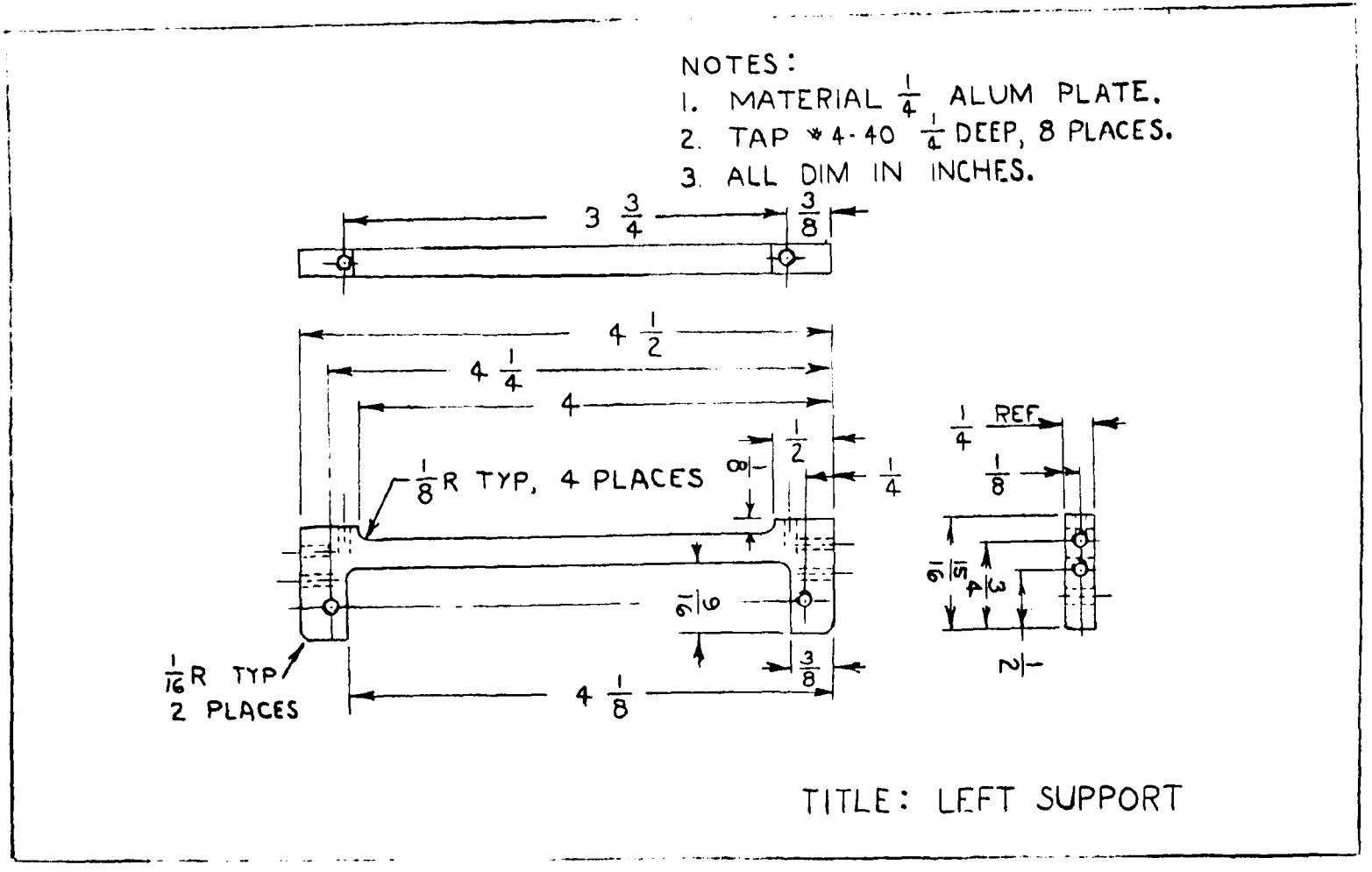


Figure 11. Flight Recorder Mechanical Drawings, Sheet 3 of 6

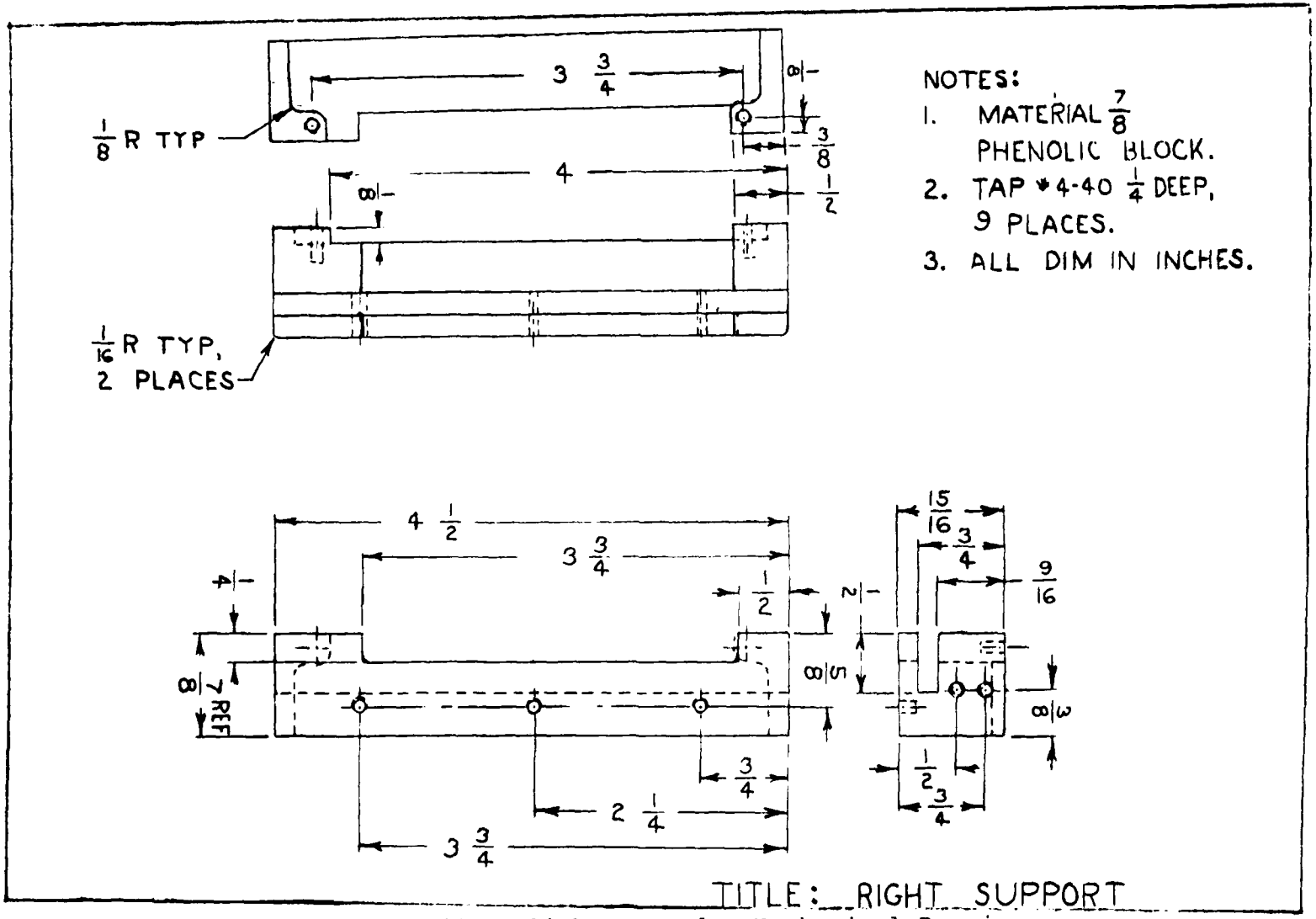


Figure 11. Flight Recorder Mechanical Drawings, Sheet 4 of 6

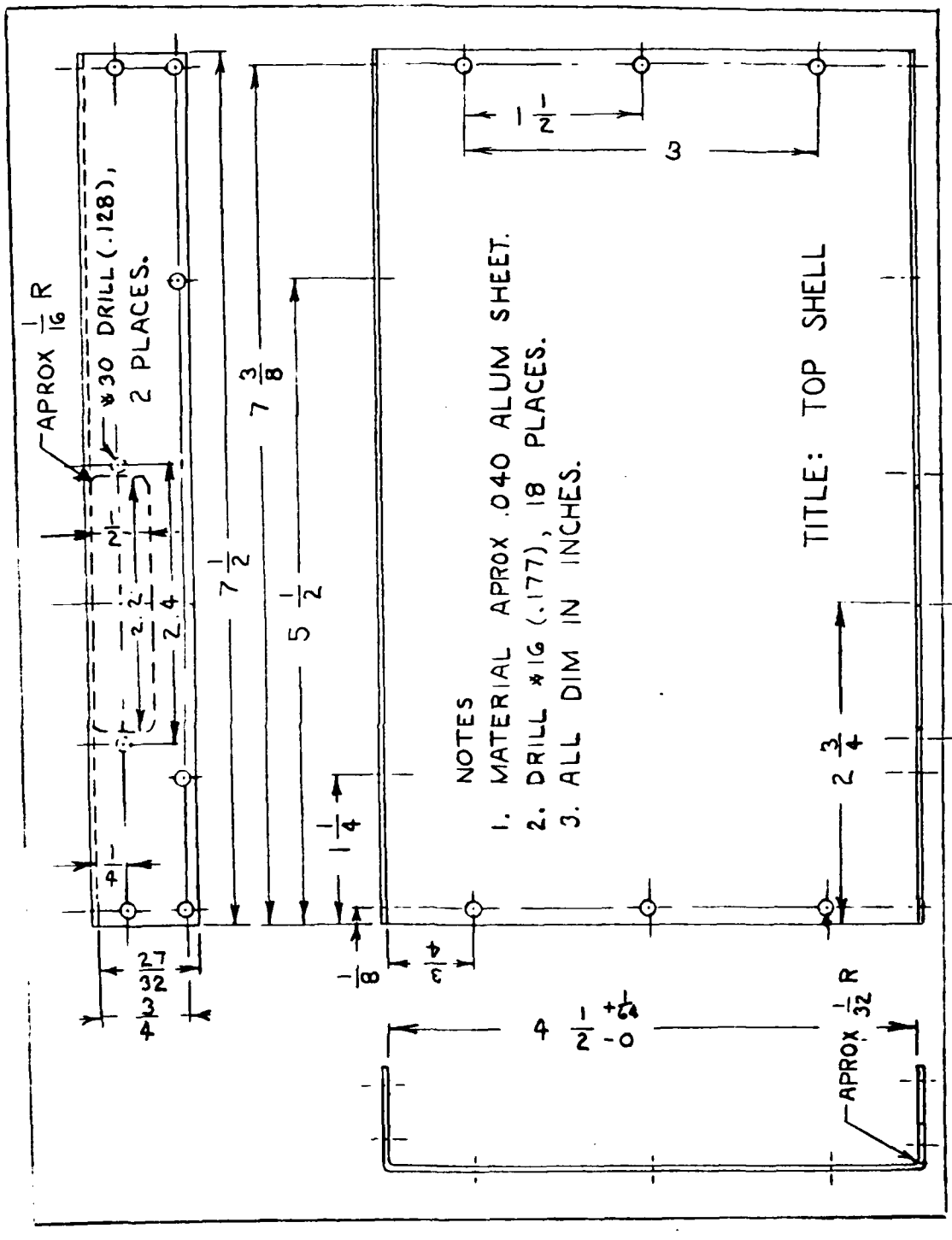


Figure 11. Flight Recorder Mechanical Drawings, Sheet 5 of 6

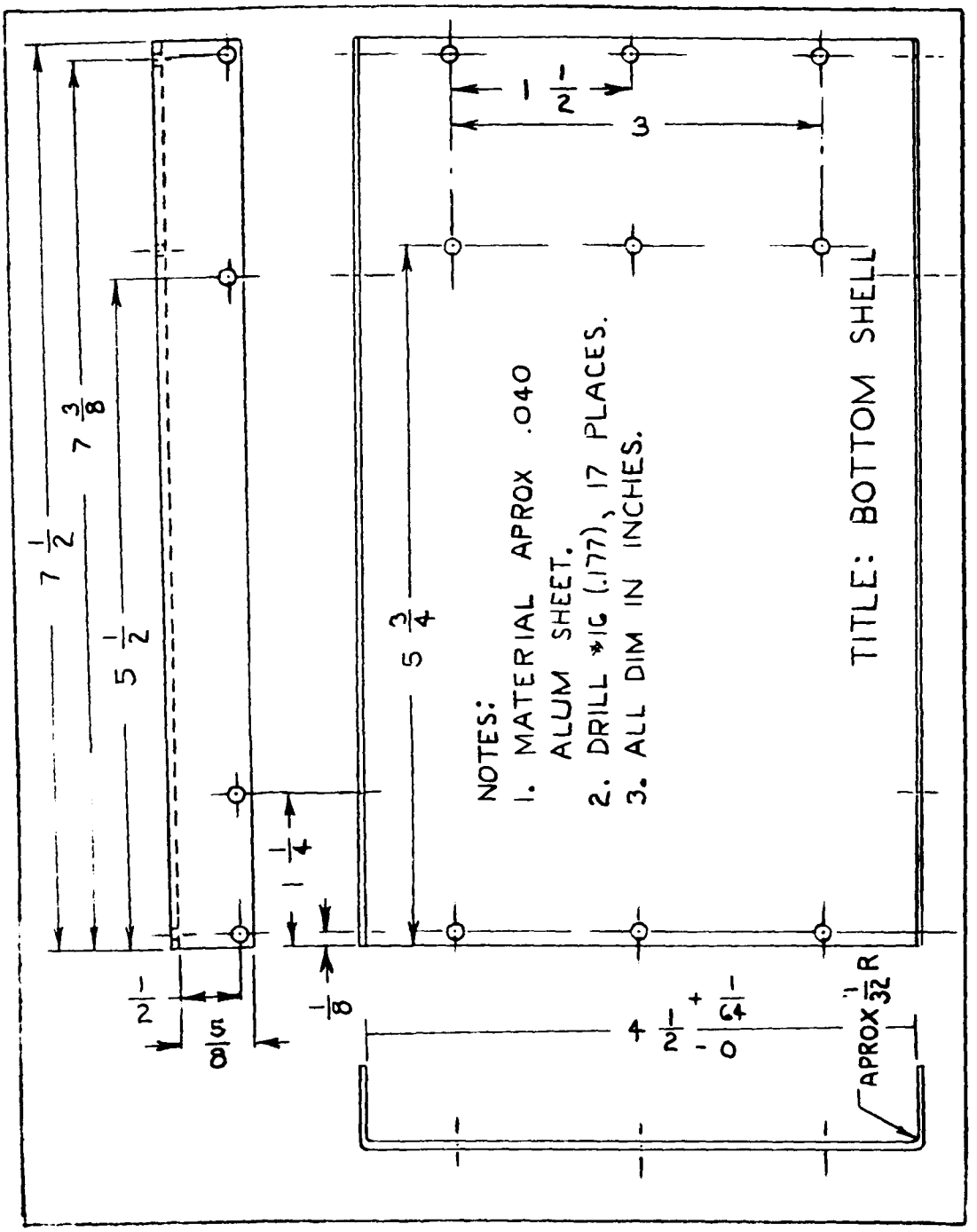


Figure 11. Flight Recorder Mechanical Drawings, Sheet 6 of 6

IV Design Evaluation

Introduction

Physical design is a synthesis process in which designers apply creative thought to their acquired knowledge to conceptualize the final product. The design process can be helped by logical thought and effort, but the final concept may come in an instant of insight. Yet, designers would be deficient if they did not continue to improve and refine their product during the periods after product conception. Once a design has been built in hardware, the designer needs feedback to determine to what extent the design meets the system requirements.

Physical design consists of the simultaneous satisfaction of a myriad of conflicting requirements. For example, the recorder shall be of small physical size, yet the recorder needs space for memory storage devices and batteries so that it can function for long periods. The conflicting requirements that must be satisfied in a physical design are too complex to be optimized by a computer algorithm; rather, the requirements are mutually satisfied (not optimized) by the human designer who is aided by information derived from test and evaluation efforts.

Evaluation of the product through a logical series of inspections and tests provides data which discloses the extent to which the preliminary design analyses were correct. Since analyses are mathematical models, they are imperfect and the evaluation data determines to what extent

the models are suitable. Physical design is a complex process, and test data may disclose improvements which can be built into the product design. Evaluation can verify that all the systems requirements are met, such as the design is rugged, reliable, and safe.

Test Plan

The test program consists of a series of visual inspections, electrical tests, and mechanical tests which demonstrate the extent to which the design meets the system requirements of Chapter II. The testing is conducted in an ordered sequence such that simple modules are tested first. Then, the simple modules of a subsystem are tested together to demonstrate the function of the system. Finally, all subsystems are tested together to demonstrate the total recorder.

Evaluation begins with a visual inspection of all components and comparison with their plans. Electrical function of electronic components are verified by installing them in the recorder breadboard. The circuit board is inspected with the aid of a continuity tester. The inspector notes the quality of the processing and visually observable errors.

Electrical Tests

The Intel magnetic bubble memory board is assembled and its electrical function demonstrated in the recorder breadboard. The microprocessor circuit board is assembled and an ohmmeter check is made across power and ground lines. A program is loaded into the EEPROM module which exercises

the hardware with a series of tests which command each hardware function in turn. The program in these EEPROMs give the recorder a built in test capability. The test program has been published (15:69-84), and an improved version has been written (30). The operator observes the proper output from an NSC810 RAM/IO/Timer port as each function test is complete. Because of the speed with which microprocessors work, these tests are complete and yet fast. Software halts are built into the test routine for the convenience of the tester. The device is measured for RF emissions which could interfere with aircraft electrical systems. These tests verify electrical function in the laboratory.

Mechanical Tests

The recorder must perform under use conditions and testing must build confidence that it will do so; however, testing must be tempered by time, cost, and equipment availability constraints. The recorder is subjected to shock, vibration, and temperature cycling tests in order to certify that it can meet the reliability requirement. The recorder is subjected to an altitude chamber test to demonstrate that it will not explode, leak caustic material, exude poisonous gas, and the like under an abnormal flight condition.

Mechanical tests are designed to demonstrate that the designed equipment functions properly in the expected environment. The military has many years experience testing

electronic systems which has been researched to select suitable combinations of tests and extremes. The procedures and conditions defined in MIL-E-5400T and MIL-T-5422F have been used as guides and modified as appropriate to produce an applicable series of tests.

Temperature Altitude. Combining temperature and pressure extremes induce electrical, thermal, and pressure stress concurrently in the equipment and accelerate the incidence of infant mortality problems. The temperature extremes have been selected for the Intel 7110 bubble memory.

Test Procedure. The recorder without the battery pack is placed in a test chamber, making connections for power and instrumentation as necessary so that proper recorder operation can be verified.

With the recorder not operating, the chamber conditions are adjusted to -40 degrees C at atmospheric pressure. The condition should be stablized for two hours.

With the recorder not operating, adjust the chamber conditions to 0 degrees C at one atmosphere. After the chamber conditions have stabilized, the recorder is turned on and satisfactory operation is verified. The recorder is turned off and the chamber is again stabilized at 0 degrees C. Then the recorder is operated again. This step is repeated a third time.

With the recorder not operating, the chamber is stabilized at 0 degrees C. Then the recorder is turned on and the altitude adjusted to 10,000 feet. Upon reaching

altitude, the recorder is turned on and satisfactory operation is verified.

With the recorder not operating, adjust the chamber conditions to 85 degrees C at one atmosphere, and let the chamber stabilize for 16 hours. At the conclusion of this period, the recorder is visually inspected. With the recorder not operating, the chamber temperature is lowered to 70 degrees C. When the temperature has stabilized, the recorder is operated for four hours and satisfactory operation is verified.

Vibration. Vibration testing discloses fatigue failure modes and resonant frequencies in the equipment design. Vibration tests for the recorder include both frequency sweeping and resonant frequency dwell.

Test Procedure. The recorder is attached to a vibration table in an orientation selected by the tester. Connections are made for instrumentation as necessary. A survey for resonant frequencies is conducted by slowly varying the recorder through the frequency range of 60 Hz to 2000 Hz at ± 2 g of maximum force. The recorder is operated and visually and aurally checked for any frequency-dependent mechanical disturbance. If any resonant frequencies are detected, the recorder is vibrated for 30 minutes at ± 2 g at each resonant frequency.

Next, the recorder is subjected to a cycling vibration test. The recorder is vibrated at ± 2 g while the frequency is swept logarithmically from 60 to 2000 Hz over a period of

90 minutes. At the conclusion of this period, the recorder is electrically checked for satisfactory performance, and visually checked for evidence of mechanical failure. The cycling test is repeated twice more with the recorder oriented along each of the two remaining major axes.

Shock. All equipment is subjected to bumps while being transported, bench tested, and operated. The shock test builds confidence in the structural integrity of the recorder.

Test Procedure. The recorder is mounted to a shock machine. Three shocks in each direction are applied along each of the three major axes for a total of 18 shocks. The shocks are roughly sinusoidal in shape with a maximum amplitude of 10 g and a duration of 10 milliseconds. At the conclusion of the test, the recorder is electrically checked for satisfactory performance and visually checked for evidence of mechanical failure.

Field Failure and Maintenance Information

A test program is a simulation of the expected use, but it never matches a real use situation. The constraints of time, cost, and equipment availability dictate that this be so. The actual history of equipment use in the field provides data that can be used to mature product design. The data from field use is collected through a coordinated program of trouble reporting and subsequent failure analysis (1:381).

These last four chapters have logically followed the design of the recorder from a rough requirement to a tested product. The next and final chapter discusses the extent of the effort, lists those lessons learned from the task, and recommends areas for future study.

V. Conclusions and Recommendations

Conclusions

This thesis has conceptualized the physical design of the flight recorder and defined the detail design. The flight recorder has been carried from a wire wrapped bread board to a true prototype unit. The requirements were that the flight recorder be solid state, microprocessor controlled, unobtrusive, and battery operated. All four of these requirements have been met; however, final battery selection is currently open.

The battery selection depends on experience with the flight recorder and safety analysis. An important factor in battery drain is the frequency of MBM read and write operations. This factor is a direct function of software, and software development is needed which minimizes power requirements. Software affects memory requirements, too.

The MBM contained in the prototype holds one million data bits. It is felt that good software can do a lot with this amount; however, a second MBM board can be easily packaged and connected to the flight recorder through a connector on the left end plate. The electrical interface is very straight forward and is listed in the Intel literature.

A second approach to increased MBM storage is a more dense MBM package. Intel is currently producing four megabit MBMs for sampling, and these MBMs fit in the same physical space as the current ones. Thus, the flight

recorder has been built with a less than one megabyte capacity, but the design remains modular to accomodate the new MBMs and to await memory-thrifty software development.

The flight recorder cannot be maintained without front panel support, and the IR Debugging Tool developed by Meisner (15:236-255) provides support for software development. With the proper interconnection cable to the microprocessor board bus connector, the IR Debugging Tool is fully compatable with the flight recorder.

A thesis is an academic experience which produces intellectual conclusions. The main conclusion in this reguard is the fact that concerns about cost, schedule, and part delivery took much more time than was anticipated, and schedule and availability of parts had a greater impact on design that the elegance of the approach. The student struggled mentally for the "best" way, but in the end the design was driven by pragmatic considerations.

Recommendations

The flight recorder has been designed and built; however, the unit must be tested using the information in Chapter IV as a guide. With the flight recorder complete, investigation should turn to software development. Software should be developed which minimizes memory and battery requirements.

Next, a system should be developed for a field processing capability for the recorder. The system should verify that the recorder is operating properly at the last

AD-A127 304 A PORTABLE PHYSIOLOGICAL DATA RECORDER USING MAGNETIC BUBBLE MEMORY(U) AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OH SCHOOL OF ENGINEERING G R SIMS

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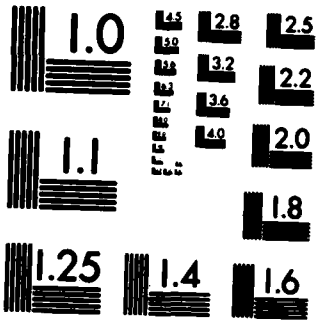

possible time before an expensive aircraft sortie is launched. Then, a system should be developed to move the stored data from the MBM into the laboratory computer. Finally, a system should be developed which would allow the laboratory personnel to program the recorder using a high order computer language such as basic. With these additions, the flight recorder would become a flexible data acquisition system and integrate fully with the current IFPDAS hardware and procedures.

Bibliography

1. "Battery." Van Nostrand's Scientific Encyclopedia, fifth ed. 1976.

2. Carter, Harold. Various unpublished works. Wright-Patterson AFB OH: School of Engineering, Air Force Institute of Technology. 1982.

3. "CMOS 8-BIT Microprocessor." EDN Magazine. 27:192 10 Nov 82.

4. Cohen, Danny and Vance Tyree. "Quality Control from the Silicon Broker's Perspective." VLSI Design, 3:4, 24-30 (July,August 1982).

5. Cummins, S.E. Improved Reliability Prediction Model for Field-Access Magnetic Bubble Devices. Report AFWAL-TR-81-1052. Air Force Avionics Laboratory: Wright Patterson AFB OH, October 1981.

6. Everitt, William L. Physical Design of Electronic Systems. Volume 4, Design Process. Englewood Cliffs, N. J.:h Prentice-Hall, 1972.

7. Glaser, Arthur B. and Gerald E. Subak-Sharpe. Integrated Circuit Engineering. Reading, MA: Addison-Wesley, 1979.

8. "Hermetic Chip Carrier Packaging." High Reliability Integrated Circuits. Somerville, NJ: RCA Solid State Division. Databook Series SSD-230A: 1982.

9. Hill, Robert E. Aircrew Modularized Inflight Data Acquisition System. MS Thesis. Wright-Patterson AFB OH: School of Engineering Air Force Institute of Technology, December, 1978.

10. IC Master. Hearst Business Communications, Inc. Garden City NJ. 1982.

11. IC Memories. Hitachi catalogue HLN100. Circa 1982.

12. Intel Military Intelligence. Chandler AZ: Intel Corp. 2:1. Second quarter, 1982.

13. Jolda, Joseph G. and Stephen J. Wanzek. Aircrew Inflight Physiological Data Acquisition System II. MS Thesis. Wright-Patterson AFB OH: School of Engineering, Air Force Institute of Technology, December 1977.

14. Mead, Carver and L. Conway. Introduction to VLSI Systems, second printing. Reading, MA: Addison-Wesley, 1980.

15. Meisner, Robert E. An Inflight Recorder Prototype for the Inflight Physiological Data Acquisition System III. MS Thesis. Wright-Patterson AFB OH: School of Engineering, Air Force Institute of Technology, March 1982.

16. Military Handbook Reliability Prediction of Electronic Equipment. MIL-HDBK-217D. Griffiss AFB NY: Rome Air Development Center. January 15, 1982.

17. Military Specification Electronic Equipment, Aerospace, General Specification for. MIL-E-5400T. Lakehurst, NJ: Navel Air Engineering Center, 5 Sep 1980.

18. Military Specification Testing, Environmental, Airborne Electronic and Associated Equipment. MIL-T:5422F. 30 Nov 71.

19. Moore, Kenneth L. Aircrew Inflight Physiological Data Acquisition System. MS Thesis. Wright-Patterson AFB OH: School of Engineering, Air Force Institute of Technology, June 1980.

20 Shackford, Joanne. Personal Interview. USAFSAM, Brooks AFB Tx, 18 January 1982.

21. Shackford, Joanne. "An Inflight Physiological Data Acquisition and Analysis System." Unpublished article. Crew Technology Division, USAFSAM, April 1981.

22. Skorup, Gordon E. SOS COS/MOS Universal Array User's Manual. RCA Solid State Technology Center. Somerville NJ: 1980.

23. Smith, Robert P. "Mead-Conway: A Method for Systems in Silicon," Computer Design, 21:5, 221-5 (May, 1982).

24. Sze, S. M., Physics of Semiconductor Devices, Second Edition, NY: John Wiley & Sons (1981).

25. Trimberger, Stephen. "Automating Chip Layout," IEEE Spectrum, 19: 38-45 (June 1982).

26. Trivedi, Kishor S. Probability and Statistics with Reliability, Queuing, and Computer Science, Applications. Englewood Cliffs, NJ: Prentice-Hall, 1982.

27. The TTL Data Book. Dallas TX: Texas Instruments, Inc. 1981.

28. Walker, Rob, Richard Derickson, and Keith Lobo. "CMOS Logic Arrays: A Design Direction," Computer Design, 21:237-245 (May 1982).

29. Walsh, Bill. "The Promise of Fiber Optics," Air Force Magazine, 64: 42-46 (July 1981).

30. White, Anthony. Various unpublished works. Wright-Patterson AFB OH: School of Engineering, Air Force Institute of Technology, 1982.

Vita

Grover Raymond Sims entered the Virginia Polytechnic Institute and State University in September 1962 and earned the Bachelor of Science in Electrical Engineering (B.S.E.E.) degree. After graduation, he worked for Texas Instruments, Inc., where he designed circuits used in the terrain following radar for the A7-D and -E aircraft. The next year he entered the Air Force and was commissioned in August 1968. Upon commissioning, he worked as a reentry systems engineer on the Safeguard Test Targets Program at Vandenburg AFB CA. In this position, he was responsible for the final assemble, checkout, and launch of R&D payloads. In January 1972, he was reassigned to the Traffic Control and Landing Systems System Program Office, Hanscom AFB MA. While at Hanscom he served as test programs manager for various items of equipment such as airborne TACAN sets, air traffic controller equipments, and en-route navigation aids. From March 1975 to June 1981, he served tours as an Air Training Command instructor and an AF Manpower and Personnel Center personnel manager. He earned the Master of Arts degree in Management from Webster College MO in 1978. He entered AFIT, School of Engineering, in June 1981.

Permanent Address: 7351 Union Schoolhouse Rd
Dayton OH 45424

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19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Inflight Physiological Data Acquisition System (IFPDAS)
Complementary Metal-Oxide Semiconductor
Electrically Erasable Programmable Read-Only memory
NSC-800 microprocessor, Microcomputer, Remote DataAcquisition

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Text documents the physical design of a man-portable digital data acquisition system. Work includes schematics and detail part drawing. The design is essentially a single board computer featuring all CMOS parts. Secondary storage is on a mixed technology board which includes an Intel 7110 magnetic bubble memory device.

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